CMOS Direct-Injection Divide-by-3 Injection-Locked Frequency Dividers

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***Abstract*—This paper proposes CMOS LC-tank divide-by-3 injection locked frequency dividers (ILFDs) fabricated in 0.18 μm and 90nm CMOS process and describes the circuit design, operation principle and measurement results of the ILFDs. The ILFDs use two injection series-MOSFETs across the LC resonator and a differential injection signal is applied to the gates of injection MOSFETs. The direct-injection divide-by-3 ILFDs are potential for radio-frequency application and can have wide locking range.**

***Keywords*—LC-tank; divide-by-3 injection-locked frequency divider; direct-injection; locking range; CMOS.**

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1 Introduction

Frequency dividers (FDs) are widely used for sub-blocks of phase locked loop (PLL) and carrier recovery blocks. A popular FD is the LC resonator based injection-locked frequency divider (ILFD) because the operating frequency can be very high and the divider consumes low power. They are free-running oscillators which lock in phase and frequency to an injected input signal. When the incident frequency is a harmonic of the oscillation frequency, frequency division is performed. The even-modulus ILFDs include divide-by-2/4 and the odd-modulus ILFDs include divide-by-3 circuits. Figure 1 shows the series-injection divide-by-3 ILFD [1, 2]. Figure 2 shows the parallel-injection divide-by-3 ILFD [3]. Figure 3 shows the direct-injection divide-by-3 ILFD [4]. The direct injection method can be used for higher frequency operation than the tail injection method. However, the

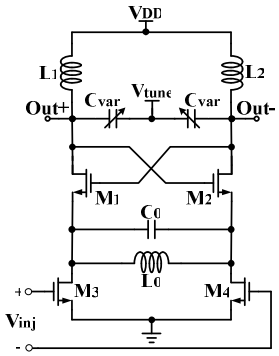

Fig. 1. Schematic of the series-injection divide-by-3 ILFD.

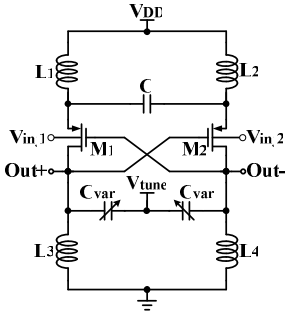

Fig. 2. Schematic of the parallel-injection divide-by-3 ILFD [3].

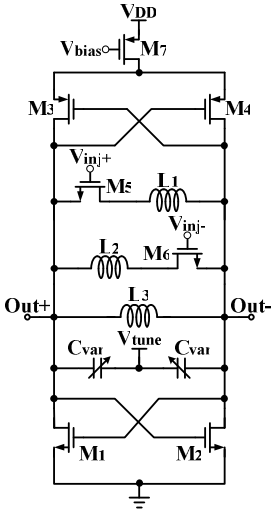

Fig. 3. Schematic of the direct-injection ILFD [4].

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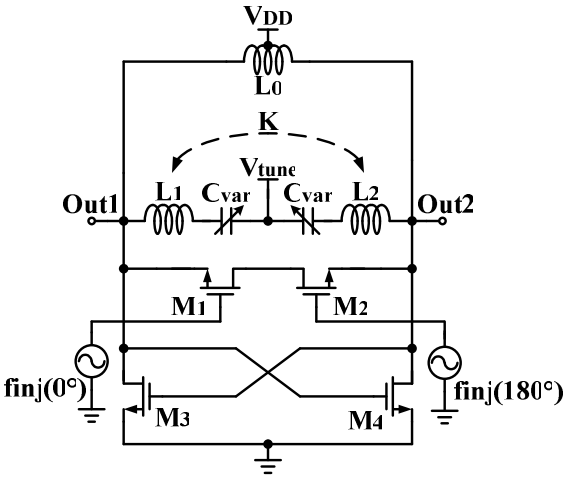

Fig. 4. Schematic of the studied direct-injection divide-by-3 injection-locked frequency divider.

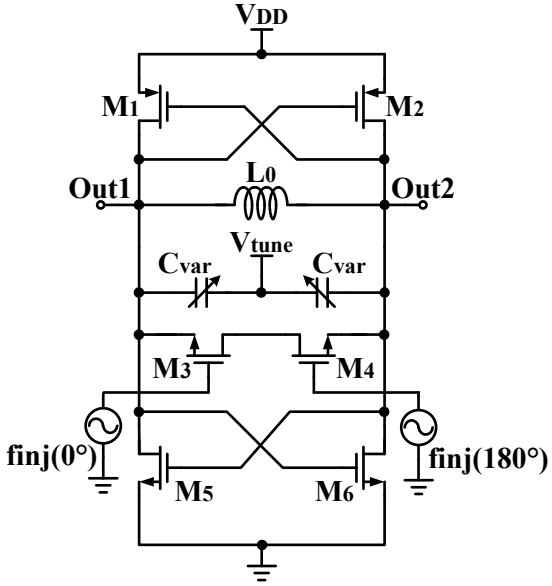

Fig. 5. Schematic of the direct-injection ILFD.

tail injection method uses stacked MOSFETs and is not a good option for low-voltage application as compared with the direct injection method.

The direct-injection method shown in Fig. 3 uses two inductors increase the die area and product cost. This paper proposed new direct-injection divide-by 3 ILFD for small die area. The organization of the paper is as follows. Section II gives a description of the circuit design and operation principle of the circuit, and then the measurement results are presented in Section III.

2 Circuit Design

The circuit diagrams of the studied divide-by-3 ILFD circuits are shown in Fig. 4 and 5. In Fig. 4, The ILFD circuit is a cross-coupled VCO with two injection MOSFETs, a pair of varactors Cvar is used for frequency tuning, and it forms the resonator with the inductors (L0~L2). The voltage Vtune is used to tune the capacitance of varactors and the oscillation frequency. The injection MOSFETs (M1, M2) with dc gate bias Vinj are used to couple the injection signal to the LC resonator.

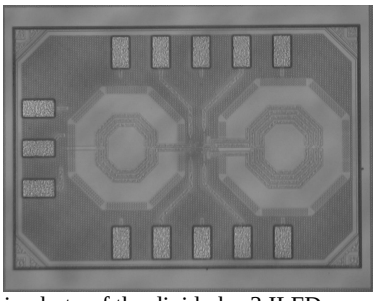

Fig. 6(a). Chip photo of the divide-by-3 ILFD.

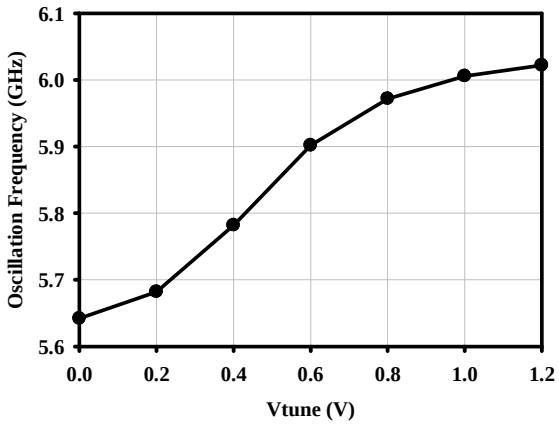

Fig. 6(b). Measured free-running frequency tuning range of the proposed divide-by-3 ILFD circuit. V_{DD} = 0.5 V, and Vinj = 0.5 V.

In Fig. 5, the ILFD circuit is a double cross-coupled VCO with two injection MOSFETs, a pair of varactors Cvar is used for frequency tuning, and it forms the resonator with the inductor L0. The voltage Vtune is used to tune the capacitance of varactors and the oscillation frequency. The injection MOSFETs (M3, M4) with dc gate bias Vinj are used to couple the injection signal to the LC resonator. The p-type transistors (M1, M2) and the n-type transistors (M5, M6) are used to generate the negative resistance to compensate for the tank loss.

3 Measurement and Discussion

The proposed circuit shown in Fig. 4 has been implemented in the retrograde twin-well TSMC 90nm 1P9M CMOS technology and the chip photo of the ILFD is shown in Fig. 6(a), where one center-tapped inductor and one transformer are shown on the left and right hand sides respectively. The die area of the chip with is 0.601 × 0.858 mm^2. The measured tuning range is shown in Fig. 6(b). The tuning range of the ILFD is from 5.642 to 6.022 GHz at V_{DD} = 0.5 V. As the gate voltage of the varactors increases, the varactor's capacitance decreases, therefore the

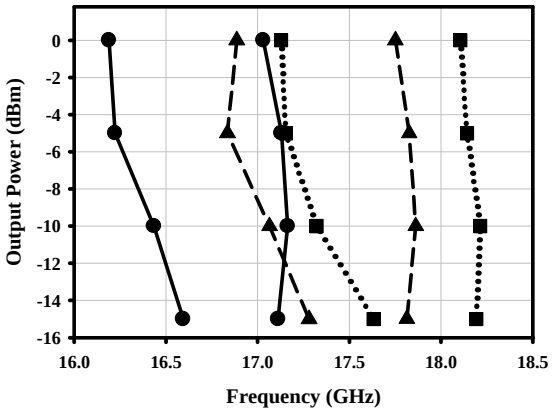

Fig. 6(c). Measured input sensitivity of the ILFD with 3 division ratio. V_{DD} = 0.5 V, Vinj = 0.5 V and Vtune = 0.0, 0.5 and 1.0 V from the left to the right.

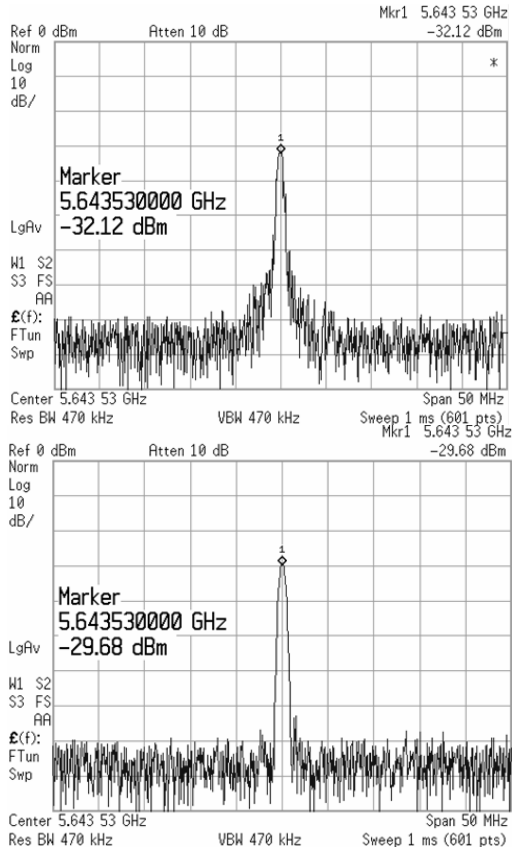

Fig. 6(d). Measured free running (top plot) and locked (bottom plot) spectra of the ILFD in the divide-by-3 mode. V_{DD} = 0.5 V, Vinj = 0.5 V, finj = 16.93 GHz.

oscillation frequency increases. Figure 6(c) shows the measured relationship between input sensitivity and operating frequency of the ÷3 ILFD under the condition of incident power Pin = 0 dBm, Vtune = 0.0~1.0 V and V_{DD} = 0.5 V, with a total operation locking range is 1.91 GHz, from 16.19 to 18.105 GHz. Figure 6(d) shows the measured output spectra of the divider before and after the locked conditions in the ÷3 mode. The locked output spectra show a lower phase noise. The ILFD can track the low-phase-noise of injection source.

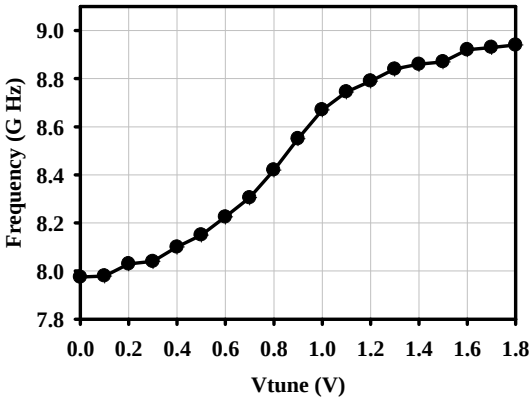

Fig. 7(a). Measured tuning range by varying Vtune of varactor. V_{DD} = 1.8 V.

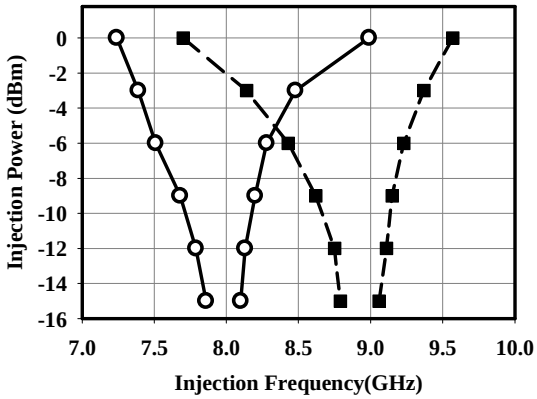

Fig. 7(b). The locking range of ILO. V_{DD} = 1.8 V, Vinj = 1.25 V, Vtune = 0 V and 1.8 V.

Tab.1 Comparison of ÷3 injection-locked frequency dividers

Ref.	Tech. (μm)	Pin (dBm)	V_{DD} (V)	Pdiss. (mW)	Operation Range (GHz)
[2]	0.18	4	1.8	4.59	16.7 ~ 17.7
[3]	0.35	10	1.5	15.15	6.9 ~ 8.4
[4]	0.18	0	1.8	4.97	15.04~ 17.12
This	0.18	0	1.8	5.4	25.5 ~ 30.3
This	0.09	0	0.5	2.63	16.19~18.105

The LC tank ILFD shown in Fig. 5 have been designed and fabricated in the TSMC 0.18 μm CMOS technology. Figure 7(a) shows the measured tuning curve of the first-harmonic ILO by varying the varactor's tuning voltage at Vinj = 1.25 V. The free-running tuning range is from 7.97 GHz to 8.94 GHz. The locking range is affected by the dc bias Vinj of M3 and M4. An optimum Vinj of 1.25 V is obtained for maximum locking range under a fixed injection power. Figure 7(b) shows the operation frequency and locking range dependence on input power for the first-harmonic injection-locked oscillator biased at V_{DD} = 1.8 V and Vinj = 1.25 V while varying Vtune. An external injected signal power of 0 dBm provides a total locking range of 7.24 to 9.57 GHz. We simulated the operation frequency (Continued on P.128)

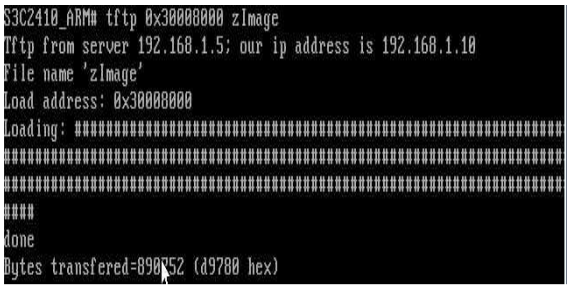

Figure 4 linux's running

6 Conclusion

After that steps we can see the kernel can run stablly on the S3C2410. We adopt an easy way to port linux to S3C2410.For the reason that the method we adopt has both less complexity and high effciency so it will give help to our embedded development.

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(From P.120)

range of divide-by-3, it's from 25.5 to 30.3 GHz. The experimental data for divide-by-3 ILFD is not available at the present time. Table 1 shows the comparison between our presented injection-locked dividers and other ILFDs.

4 Conclusions

CMOS direct-injection divide-by-3 frequency dividers have been proposed and implemented in the 0.18um 1P6M CMOS and 90nm 1P9M CMOS technologies. The operation principle of the ILFDs has been described. And measurement results have been presented. Measurement data shows that the direct-injection divide-by-3 ILFD is potential for RF system applications.

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