Design and implementation of high speed TDI CCD timing-driven circuits

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Abstract: The time delay integration charge coupled device (TDI CCD) is the key component in remote sensing systems. The paper analyzes the structure and the working principles of the device according to a customized TDI CCD chip. Employing the special clock resources and large-scale phase locked logic (PLL) in field-programmable gate arrays (FPGA), a timing-driven approach is proposed, using which all timing signals including reset gate, horizontal and vertical timing signals, are implemented in one chip. This not only reduces printed circuit board (PCB) space, but also enhances the portability of the system. By studying and calculating CCD parameters thoroughly, load capacity and power consumption, package, etc, are compared between various candidates chips, and detailed comparison results are also listed in table. Experimental results show that clock generator and driving circuit satisfy the requirements of high speed TDI CCD.

Key words: time delay integration charge coupled device(TDI CCD); timing-driven circuit; field-programmable gate arrays (FPGA)

CLD number: TN29 **Document code**: A
Article ID: 1674-8042(2012)02-0185-06 **doi**: 10.3969/j.issn.1674-8042.2012.02.017

0 Introduction

High speed time delay integration charge coupled device (TDI CCD) has been widely used in aerial and space cameras[1,2]. Aerial and space cameras are high technology products that consist of many components and include many disciplines, such as optics, mechanics, electronics, etc. Among all the parts, TDI CCD is the key component in these apparatuses. Unlike CMOS sensors, timing-driven circuits cannot be integrated into CCD chip itself due to technical constraints, thus it needs peripheral timing generation and driving circuits[3].

Timing generation and timing-driven circuits of a high speed CCD are sets of pulses involving complex phase relationships, which affect signal noise ratio, transfer efficiency and so on. So the design of high speed CCD timing and their driving circuits is one of the key techniques for CCD data acquisition systems[4-6]. There are three traditional timing generation options for implementing CCD timing circuits. They are timing core in ADC chip[7], ASIC timing generation chips from Philips and other corporations[8,9] and design using CPLD respectively. Option 1 mainly aims at area CCD. For line CCD, there is seldom such type of ADC, although some products using options 2 and 3 have already achieve some success[10]. On the one hand they require significant PCB space which limits their application in compact aerial and space cameras; on the other they are not suitable for image processing which are fundamental functions in modern intelligent cameras.

There are sufficient programmable logic, IOs, high performance PLL and varieties of interfaces, such as LVDS, inside FPGA[11], so it is very suitable for implementing timing circuits. Based on a customized line TDI CCD, this paper first describes operation parameters of TDI CCD, then analyzes thoroughly issues such as practical timing constrains, PCB board requirement and power consumption encountered in practical applications[12], finally the timing circuits are implemented in one single FPGA with specific driving chips.

1 Sensor architecture

Fig. 1 shows a schematic outline of TDI sensor for one tap. The number of pixels is set to 4 096. All pixels are read out simultaneously through 8 separat-

* **Received data**: 2011-12-05
Foundation item: National High Technology Research and Development Program of China (863 Program) (No. 2009AA7010102)
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ed output registers and amplifiers (taps). Each tap serves active 512 pixels.

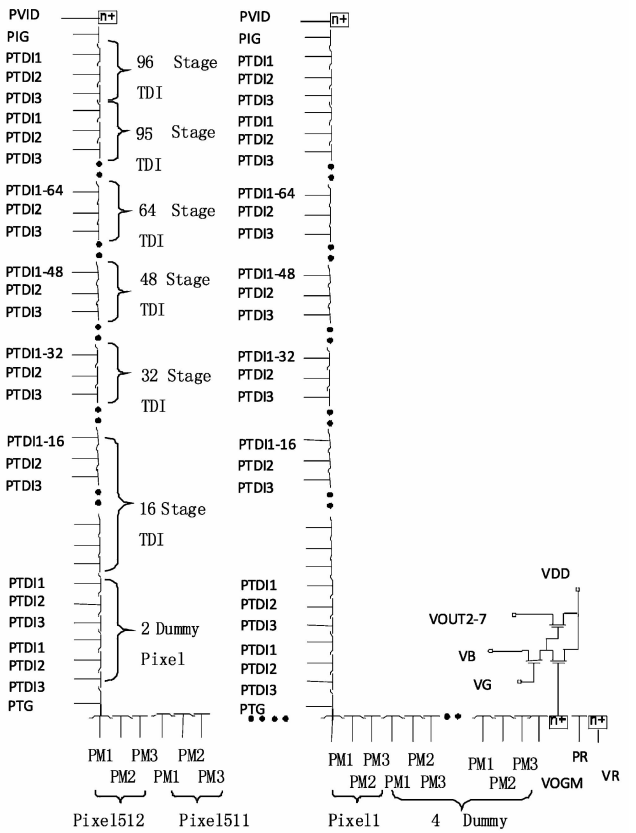

Fig. 1 Sensor architecture

The horizontal registers require 3-phase timing: PM1, PM2 and PM3. Charge is transferred pixel to pixel to the floating diffusion sense node when it produces a voltage change corresponding to the signal level. After the signal is sampled, the reset gate (PR) is clocked high to clear the signal, and restore the potential of the sense node to reset drain voltage.

The vertical image area is controlled by 3-phase timing: PTDI1, PTDI2 and PTDI3. The charge is transferred line by line in vertical direction. Finally the transfer of the image from isolation row to the readout register is controlled by PTG. To utilize the option of choosing different sensitivity levels, the TDI sensor is split in a number of stages in vertical direction. Depending on the outcome of a light measurement, the best value can be selected for capturing an image. Stage selection provides the choice of five levels of sensitivity by choosing the number of integrating lines: 16, 32, 48, 64 and 96.

2 Sensor timing and their generator

The overall timing diagram of TDI sensor is shown in Fig. 2.

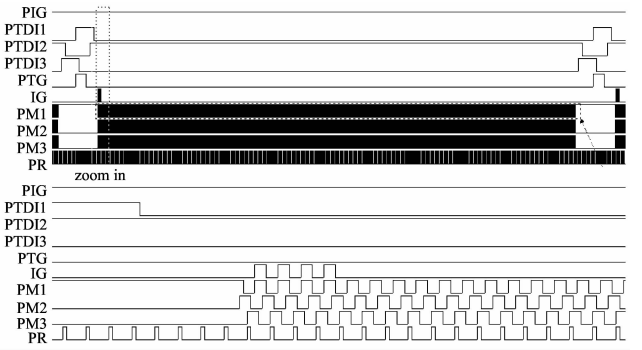

Fig. 2 Timing diagram of TDI CCD

Sensor timing block provides individual timing adjustment for:

* PM1, PM2 and PM3: horizontal clocks;
* PR: charge reset clock;
* PTDI1, PTDI2, PTDI3 and PTG: vertical clocks;
* PTDI16, PTDI32, PTDI48, PTDI64 and PTDI96: vertical clocks for stage selection.

A block diagram of TDI CCD timing circuit is shown in Fig. 3. All the four types of timing signals will be generated by FPGA, and clock oscillator will be selected to 25 MHz. Timing processing board contains three parts.

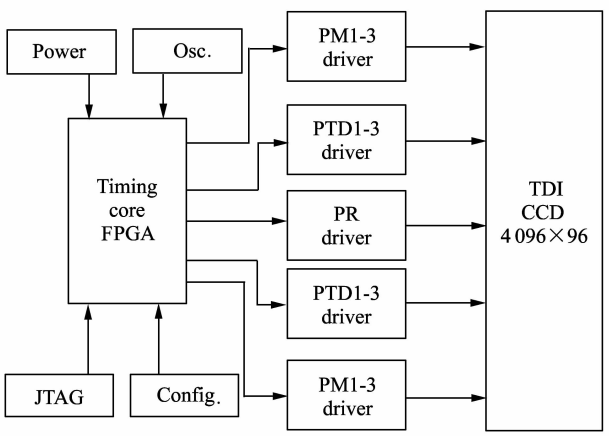

Fig. 3 TDI CCD timing-driven circuit

* Timing core inside FPGA.
* External circuitry, including oscillator, power network, JTAG interface and configuration module.
* PMX, PTDX and PR driving circuit.

2.1 Horizontal clocks generation and drivers

Horizontal registers are controlled by 3-phase clocks. Because FPGA provides flexible and complete control over clock frequency, phase shift and skew using embedded PLL, there are two options to

generate this type of timing signals. Option 1: through PLL phase delay; Option 2: multiply input clock by 6 to generate 3-phase PMX through divisions. It is expected to use LVDS oscillator to reduce jitter.

To select the PMX drivers, the following requirements are needed: 135 pF per PMX pin, 5-V swing and 25-MHz speed. PMX pins are electrically connected in the package. Aside from capacitance, the CCD sensor has series resistance on all clocks which must be accounted for proper driver and bus resistance selection. For PMX clocks, the general design guideline is that the effective RC time constant of the clock circuit should be less than 1/6 of the clock period.

For the PMX clocks, which have 7-Ω series resistance internal to the CCD, the driver plus external resistance should be less than 6.2 ns/320 pF = 19.3 Ω for a 10% design margin against errors in capacitance measurement or estimation.

According to the above analysis, 74ACT04 is selected for this design. It can be driven without logic level shifting, and its package fits into the board shape and around sensor pinout.

2.2 Reset gate timing and driving

The width of PR pulse and its timing with relation to PMX are critical to ensure an optimum output signal, because PMX initiates charge transfer into the floating diffusion. The recommended width of RST pulse is 5 ns. There are two traditional methods for implementing PR pulse. The first one is using RC time constant, in conjunction with NAND gate delay; the second one is adopting delay lines chips with NAND gate. Both of the two means occupy too much PCB area, and are short of flexibility.

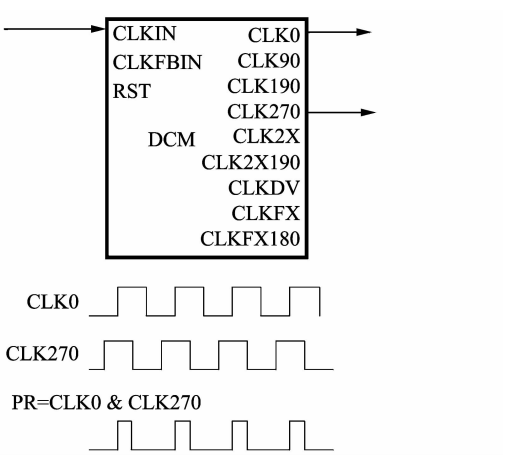

Fig. 4 Reset gate pulse generation

The digital clock management (DCM) embedded in FPGA provides an excellent method for generating precision phase-shift clock, such as 0, 90, 180 and 270 degrees. It means rising edge of the CLK0 will happen before the rising edge of CLK270 3/4 circle, which is 5 ns, NAND result of CLK0 and CLK270 is just the expected PR signal. Fig. 4 show PR generation means.

Two reset driver solutions used herein were evaluated: discrete push-pull circuit and 5-V logic integrated circuit. The following table compares both topologies.

Similar to PR driver selection, 5-V logic is selected for RST driver design. Again, it was used in previous design. It can be driven without logic level shifting, and its package fits into the board shape and around sensor pinout.

There are 2 RST sensor pins in total. Three output pins will be used to drive one sensor pin. There are 6 pins per driver package. Worst case power dissipation for the driver is

$$P_{\max} = I_{cc} \times V_{cc} + C \times V^2 \times f = 0.1\ \text{mW} + 156.65\ \text{mW} = 156.75\ \text{mW}, \quad (1)$$

where $C = 2\times26+6\times30=232$ pf, $V=5$ V and $f=25$ MHz.

2.3 Vertical timing and reverse transfer timing

Vertical timing and reverse transfer timing are relatively slow, the maximum of which is 25 kHz, so they can be implemented in FPGA easily. But one thing should be emphasized: in order to guarantee synchronization of the line scan rate and the camera movement speed, vertical timing is triggered by external signals.

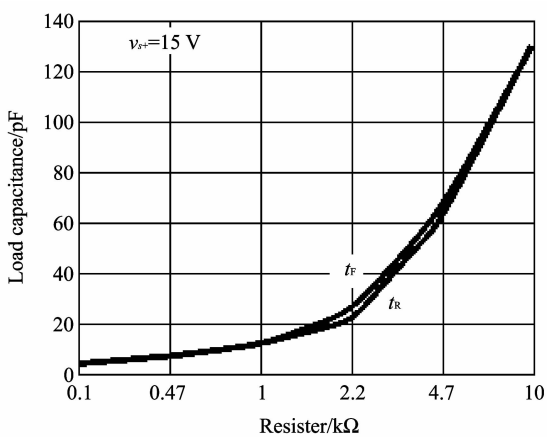

Fig. 5 PTD driver rise/fall time vs load capacitance

There are four PTD clocks and eight reversed transfer clocks. PTD pins are electrically connected in the package. Assuming 100 ns as a maximum t_R/t_F, and measured 3.8 nF worst case pin capacitance, quad-driver (option 1) with typical t_R/t_F of

40 ns is chosen. Four ICs will be used: one for PTD1-3 left, one for PTD1-3 right, and two for 8 reversed transfer clocks. Fig. 5 shows the relationship between load capacitance and rise/fall times.

To calculate total vertical clock driving power dissipation, the following values are used: 25-kHz maximum line rate, 8-V swing, and total of 24.3-nF load capacitance.

$$P_{\text{total}} = 4 \times (V_s \times I_s) + 16 \times (C_{\text{int}} \times V_s^2 \times f) + (C_l \times V_{\text{out}} \times f), \quad (2)$$

where $V_s = V_{\text{out}} = 8$ V, C_{int} is internal capacitances (80 pF, max), C_l is load capacitance (24.3 nF), I_s is quiescent supply current (3 mA from datasheet), f is the PTD frequency (25 kHz). $P_{\text{total}} = 4 \times (24$ mW$) + 16 \times (0.128$ mW$) + 39$ mW$ = 137$ mW.

To calculate the worst case PTD power dissipation, the following values are used: 25-kHz maximum line rate, 8-V swing, and total of 12-nF load capacitance (measured on 2 sensor samples).

$$P_{\text{icmax}} = (V_s \times I_s) + 4 \times (C_{\text{int}} \times V_s^2 \times f) + (C_l \times V_{\text{out}}^2 \times f), \quad (3)$$

where $V_s = V_{\text{out}} = 8$ V, C_{int} is internal capacitances (80 pFmax), C_l is load capacitance (12 nF), I_s is quiescent supply current (3 mA from datasheet), f is the PTD frequency (25 kHz). $P_{\text{icmax}} = 24$ mW$ + 4 \times (0.128$ mW$) + 19/2$ mW$ = 43.7$ mW.

The maximum allowable junction temperature is 125 ℃. Assuming that all power is dissipated through driver (which is not the case):

$$T_j = Tambient + (ThetaJA \times P_{\text{total}}) = Tambient + (43.7 \text{ mW} \times 112 \text{ ℃/W}) = Tambient + 5 \text{ ℃}, \quad (4)$$

where *Tambient* should be less than 125 ℃ − 4.9 ℃ = 120 ℃.

3 FPGA design details and experimental results

The Altera and the Xilinx FPGA are located on the sensor and processing board, respectively. They serve different purposes. The first provides all sensor clocks and interfaces with ADC and DAC. Fig. 6 provides an overview of the connections between the two FPGAs. The oscillator will be connected to the Altera FPGA, which in turn provides the Xilinx FPGA with a clock of the same frequency. However, with an input frequency of 27 MHz, less than 32 MHz, the Xilinx FPGA cannot de-skew its clock with respect to the input clock (from the Altera FPGA) using a feedback path. Hence, the two FPGAs are asynchronous and raise the following concerns.

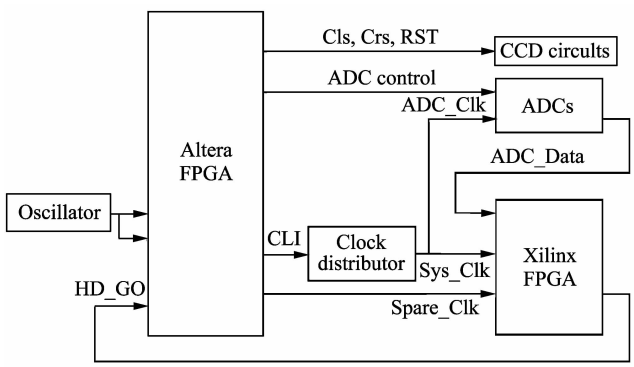

Fig. 6 Block diagram of the system

Altera FPGA generates the colcks of all sensors and ADCs required by the camera. It also interfaces with ADC and DAC. The following figure shows its block diagram.

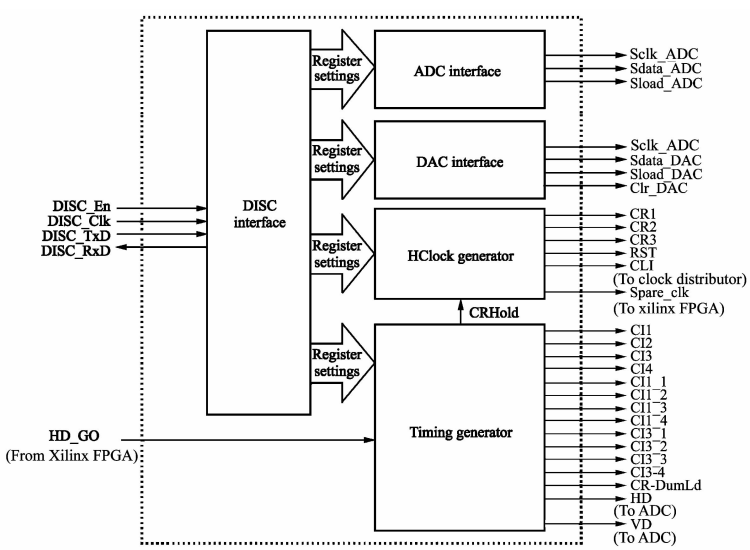

Fig. 7 Block diagram of timing circuits

The system adopts a 27-MHz external clock, which is generated by an extra oscillator. The driving sequences are produced by two counters. The shift pulse RC, and the driving pulse PMX are produced by one counter; the reset pulse RS and clamp pulse CP are produced by another counter. Table 1 shows the performance and resource usage on the FPGA.

Table 1 FPGA performance and resource usage

Parameter	Value	Max(%used)
Number of programmable logic slices	6 324	42 176(14.9%)
Number of 16-kbit RAM blocks	312	376(82.9%)
Number of global clock nets	5	32(15.6%)
Number of DCM	3	8(37.5%)
Minimum period of DSP clock	4.2 ns	7.1 ns

Then we give the signal waveforms of the CCD camera circuit with 1-GHz scope. Fig. 8 shows the phase relationship of PMX clocks. The 120 degree phase shift is clear and there is little crosstalk between the clock edges of adjacent PMX.

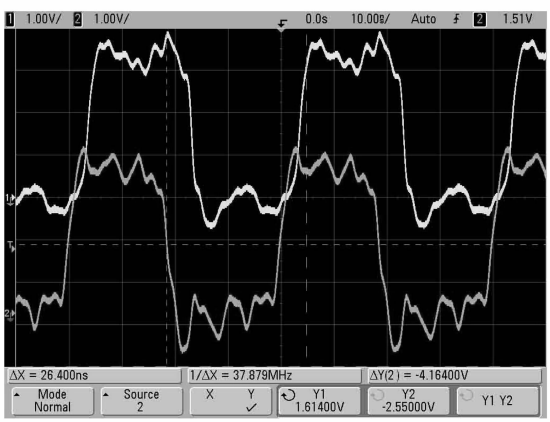

Fig. 8 Diagram of PMX timing

Fig. 9 shows the phase relationship between PR and PMX. The PR falling edge to PM1 falling edge is simultaneous, namely satisfying the requirement of the time PR rising edge to PM1 rising edge.

Two waveforms for the sensor output are plotted to show the difference in measurement using the coax verses and using an active probe on the header pin provided. The length of the scope probe cable, plus any delay in the active circuit of the probe will delay the probed signal. The plot shows about 13-ns settled video available for A/D sampling. The rising edge of PM1 is located very early in the settled video to allow the user flexibility in positioning the A/D sampling aperture.

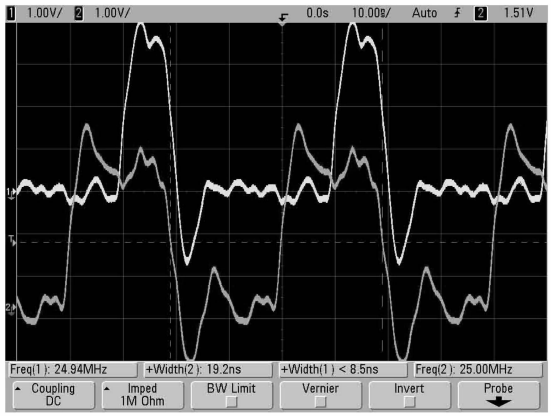

Fig. 9 Diagram of PMX and PR timing

Fig. 10 shows the relationship between PTG and PMX clocks. The PTG pulse must be positioned where the PMX clocks are not switching. 50 ns of idle clock time has been provided before and after active PTG. PTG overshoot is minimal at less than 0.5 V and there is no undershoot.

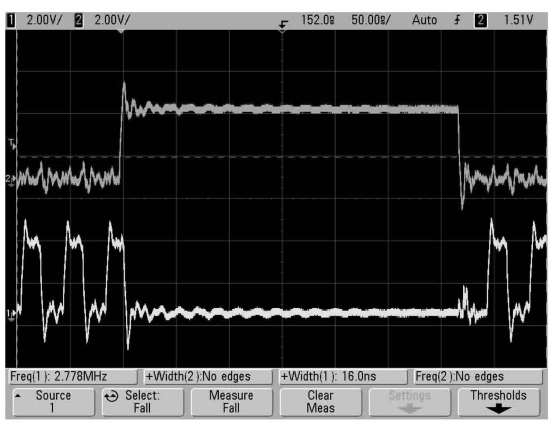

Fig. 10 Diagram of PTG and PMX timing

Using the proposed CCD timing schemes, Table 2 summarizes the test conditions.

Table 2 Testing conditions

Parameter	Test condition
Data Rate per Output/MHz	27
Illumination	Broadband with IR cut-off, or narrow band pass filters or LED's of specific wavelengths in the band pass region of each spectral zone
Data resolution/bit	8
Camera gain/dB	0
Ambient temperature/℃	20－25

And Table 3 shows the corresponding testing results.

Table 3 Testing results

Parameter	Test results
Camera line rate/MHz, max	⩾25
Camera line rate/MHz, min	⩽0.25
Horizontal CTE, per transfer	⩾0.999 95
Vertical CTE, per transfer	⩾0.999 95

4 Conclusion

TDI CCD is a special CCD sensor, which is ideally suited for application requiring high speed operation under low light level conditions for its special scanning usage. According to a costumed TDI CCD, this paper analyzes the operation parameters, such as line rate, clock frequency, etc. Then a new type of timing generator and driving circuit is developed, it functions well and shows a high flexibility. Because of its compact structure it is very suitable for application in space and aerial circumstance.

We proceed to improve our system. At first, we have many problems with the digital noise, which mainly due to a switching regulator, so we aim to design a stand-alone digital board which possesses FPGA, serial I/O, etc. Secondly, because camera link interface is widely adopted by many world leading corporations, image data will be transmitted using this protocol.

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