# Design of LED display based on FPGA

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**Abstract**：If single chip micro computer controls light-emitting diode（LED）, it needs abundant peripheral resources, but in this way, it is not convenient to be expanded, modified and maintained. In order to overcome these shortcomings, field programmable gate array（FPGA）is used to control LED. The hardware design uses low power consumption and high performance device EP1C6Q240C8. Quartus II is the software development environment. There are three modules built under the software development environment：divided clock module, word stock module and LED dot matrix display module, and these independent modules are connected to be a whole system. Finally, 32×64 dot matrix display is realized successfully. It is convenient for the customer to adjust the three independent modules according to actual demands and it is easier to realize online updation.

**Key words**：field programmable gate array（FPGA）; EP1C6Q240C8; light-emitting diode（LED）; dynamic display

With the development of economy and science, light-emitting diode（LED）has been used widely.

There are two prominent characteristics of LED dot matrix display control, one is a large quantity of data, the other is high processing speed[1]. However, the existing function of processing system is so simple that if it achieves different functions, it has to modify content through cockamamie process, which is against enhancing efficiency of development.

Now, FPGA system design has began to enter the new era of "chip programmable system", its characteristics include high density and low power consumption[2]. International companies are expanding its IP so that it can provide optimized resources and expand the market. LED dot matrix controller based on FPGA has broad application prospects[3]. It can be easily upgraded through changing FPGA internal hardware logic which can be downloaded online from the network.

Based on the above advantages, Cyclone II EP1C6 of Altera FPGA is chosen as controller to control LED dot matrix display. The main research is：

1）Hardware circuit design, including LED circuit, FPGA control circuit, power supply, etc.

2）Simulation of each module, including clock circuit, word stock and LED display, etc.

3）Based on Quartus Ⅱ development platform, by using VHDL and top design method, FPGA control circuit is realized.

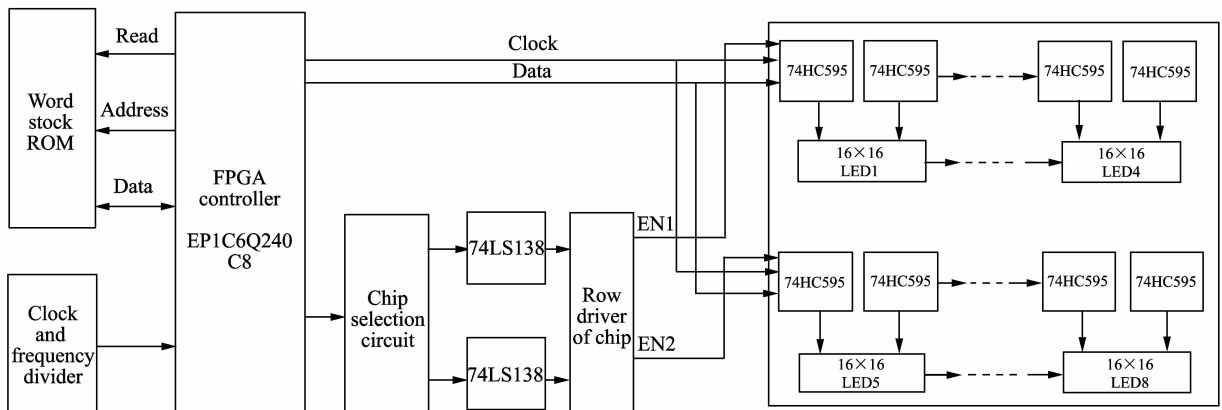The whole design diagram based on FPGA controller is shown in Fig. 1i.



Fig. 1　Design diagram based on FPGA

# 1 Design of hardware circuit

## 1.1 LED dot matrix module

In this paper, the LED dot matrix is common anode. $64 \times 32$ LED dot matrix module is got by connecting four $16 \times 16$ LED dot matrix.

The public interface serves as LED row control, and the row scanning signal can control multiple LED. Before arriving of the row scanning signal, it has to go through a driver chip — 4953[4]. Through the decoding circuit, the row scanning decides which row to display. The decoder chip is 74LS138[5]. The column scanning circuit uses the shift-register — 74HC595[6] with latch. Row control circuit of LED is shown in Fig. 2.
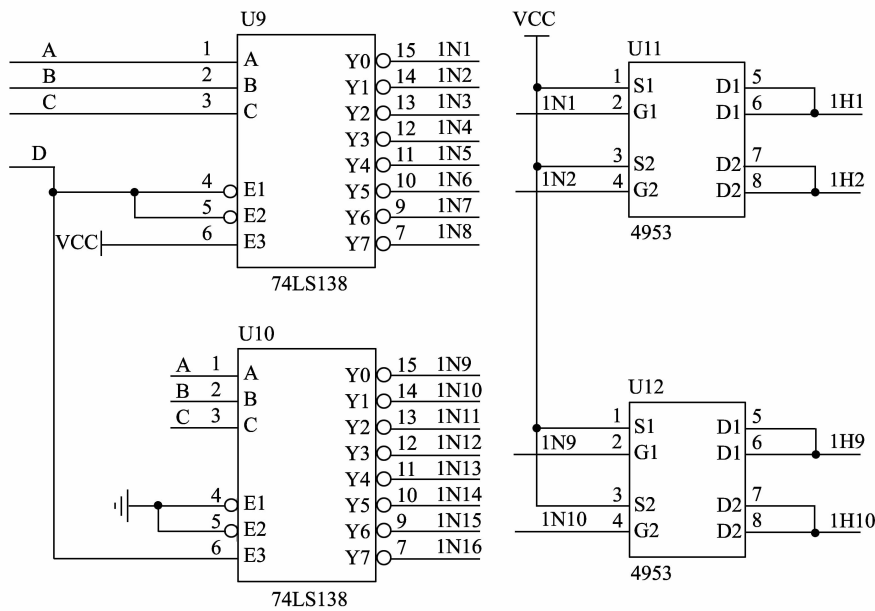


Fig. 2    Row control circuit of LED

Column control circuit of LED is illustrated in Fig. 3. Its main function is to send the word need to be displayed to LED cathode. Combining with row control circuit, LED display is realized.
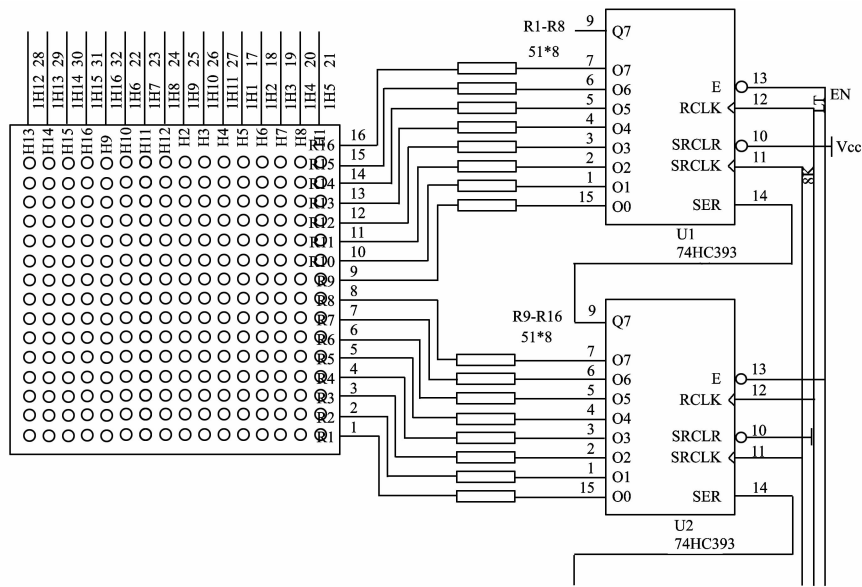


Fig. 3    Columm control circuit of LED

## 1.2 FPGA configuration circuit

The chip of Cyclone has three configuration methods[7]: active serial configuration (AS) mode, passive serial configuration (PS) mode and joint test action group (JTAG). Above three methods are de-

cided by two-bit model code, as shown in Table 1.

| MSEL1 | MSEL0 | Configuration mode |
|-------|-------|--------------------|
| 0 | 0 | AS |
| 0 | 1 | PS |
| 0 | 0 or 1 | JTAG |

In this paper, AS plus JTAG is the best choice. JTAG module is used to debug so that the program has been debugged correctly. AS module downloads the program to the chip. The chip of Cyclone supports USB cable download. One side of the cable connects the USB of PC, the other side connects circuit socket. Download speed is faster than Byte Blaster II.

## 1.3　Design of power circuit

The external power is 7.4 V. The power of FPGA I/O is 3.3 V. The power of core is 1.5 V.

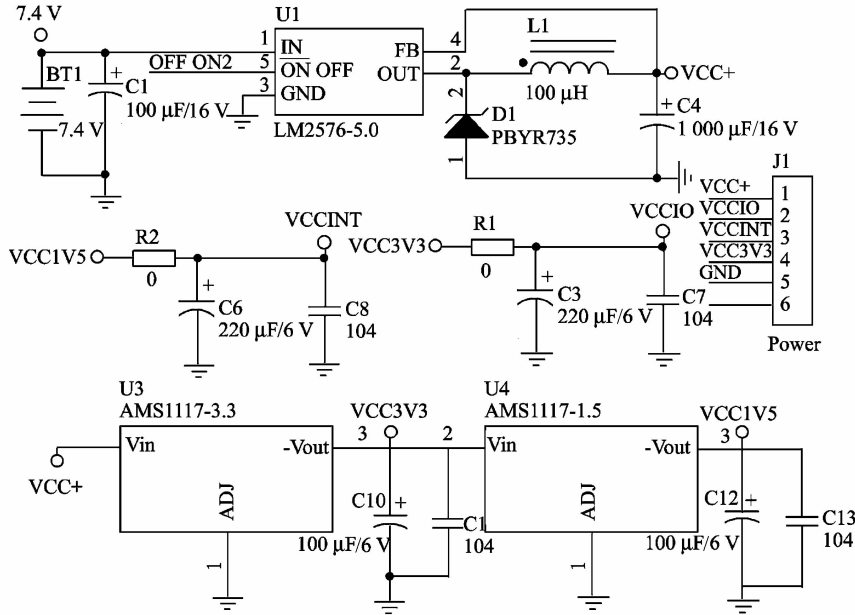In order to convert 7.4 V into 1.5 V, the circuit is designed as shown in Fig. 4.



Fig. 4　Power circuit

# 2　Software design

The design of software are consisted of five parts, this is obtaining three kinds of clock, words stock, the design of divided frequency, LED dot matrix display and system top layer design.

## 2.1　Three kinds of clock

The time sequence of row control is obtained on the basis of time sequence of 74HC595. The flowchart is shown in Fig. 5.

It is time to explain the function of the three clocks.

S_in: data shift clock.

H_clk: in order to change address of data rom and renew LED data, a rising edge is set after every eight S_in clock.

LT_in: data latch clock, after sixty-four S_in clock, set a latch and at the same time the row address adds one.
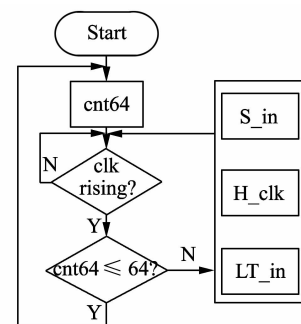


Fig. 5　Flowchart of clock

According to the above principles, in Quartus II, use VHDL to program and package a module, shading the structure of inside circuit. The clock module named My_clk is shown in section 2.5.

## 2.2　Word stock

Dot matrix display is based on glyph code. In FP-GA, LPM_ROM macro block is used for generating glyph code.

Design ideas for words stock are as follows：

1）Store 256 8-bit data in ROM.

2）Design 8-bit address pointer.

3）After eight clocks, the address pointer adds one, and read a glyph code.

The format of data of LPM‗ROM contains .mif and .hex. In this paper .hex is chosen. Contents of words stock are "山东科大 lys‗skd". The word stock module named R‗data is shown in section 2.5.

## 2.3　Design of different clock frequency[10]

When LED is in dynamic scanning, if the frequency is too high, output data may have mistakes. Conversely, if the frequency is too low, LED display is unstable. So if the frequency is controlled well, stable display characters can be realized.

In this paper, phase-locked loops（PLL）of Quartus II can achieve frequency multiplication and frequency division by setting parameters directly[9].

The divided frequency module named freq‗div is shown in section 2.5.

## 2.4　LED dot matrix display

The data of hardware circuit is output in a serial way. So data in ROM must be read bit by bit and clock signal is connected with line control signal. Characteristics of hardware circuit include：

1）The function of the shift-register.

2）Set a latch after the data has been output.

3）Control two pieces of LED dot matrix display

through changing the status of EN1 and EN2.

4）In order to display stably, once the scanning is over, then return automatic and scan again.
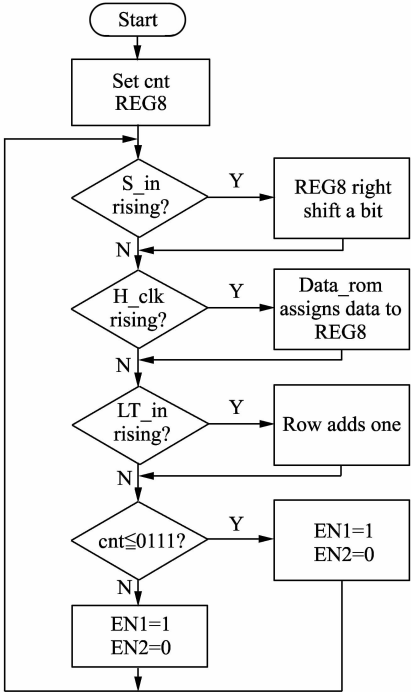
The flowchart is shown in Fig. 6.



Fig. 6　Flow chart of LED dot matrix display

The LED dot matrix display module named display is shown in section 2.5.

Fig. 7 presents the result of LED dot matrix display simulation.
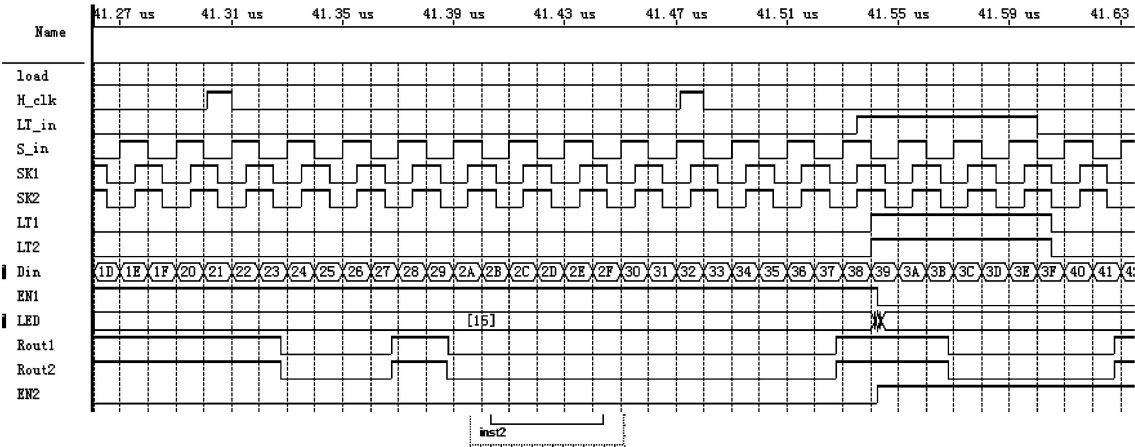


Fig. 7　Simulation results of LED dot matrix display

Load is the reset signal, and it functions in low level. Rout1 and Rout2 are the outputs of above LED and below LED, respectively, EN1 and EN2 function in high level on-off control of LED. If EN1 is in high level, the above LED functions. S‗in is assigned to SK1 and LT‗in is assigned to LT1, which function in high level. Similarly, If

EN2 is in high level, the below LED functions. S‗in is assigned to SK2 and LT‗in is assigned to LT2, which function in high level. Din is the content that is to be displayed in LED. When H‗clk is in high level, Din is read, otherwise Din is unreadable. LED decides which row is going to be displayed.

## 2.5 Top layer design of the system

Connecting the four modules above as a whole, the system design principle diagram is shown in Fig. 8.

The top layer design module is shown in Fig. 9.

Fig. 9 shows the whole software diagram, which is connected with independent modules that are generated by the previous software design. It is convenient to revise these modules, and thereby improve the efficiency.
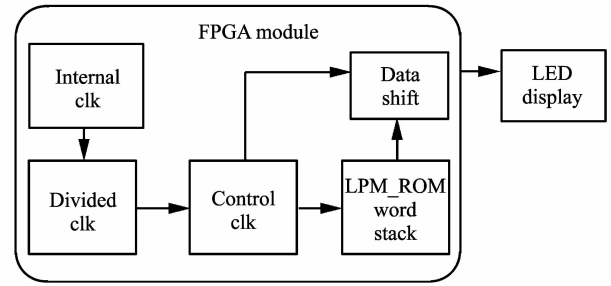


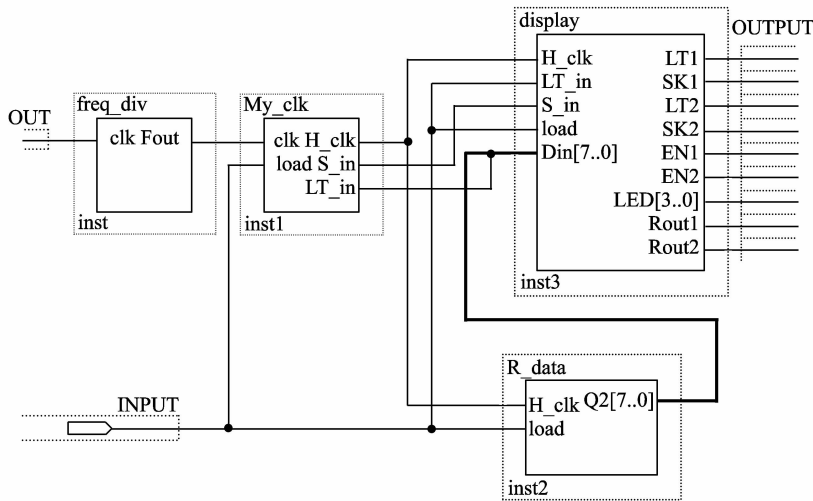Fig. 8   Module diagram of LED dot matrix display



Fig. 9   Top layer design module

Fig. 10 is the simulation results of Fig. 8. The chart shows that the timing sequence is right. Row address is controlled correctly. The simulation results is consistent with the expected.
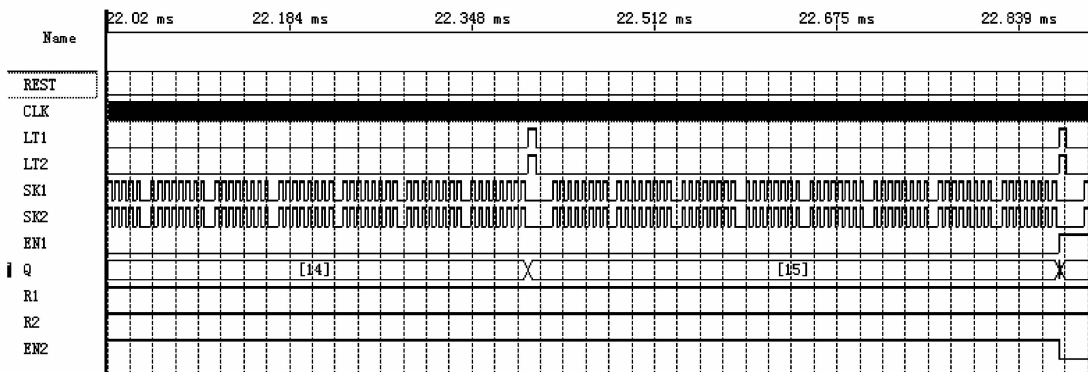


Fig. 10   Simulation results of top layer design module

# 3   Test results

Downloading the program to EP1C6Q240C8 of FPGA, the test result is shown in Fig. 11, it is the same as the expected.

# 4   Conclusion

As we know, single chip microcomputer has many advantages to control LED display[10], for example easy programming, low cost. But there are also disadvantages. When LED dot matrix is bigger, clock frequency required will be too higher to complete dynamic scan. I/O ports are used too many to achieve other functions at the same time. LED display is not stable. Realize online upgrade unfavorably.

Compared with signal chip microcomputer, FPGA could solve its shortages and optimize other functions making LED display more convenient, higher efficient. But there are several points to be paid attention to:
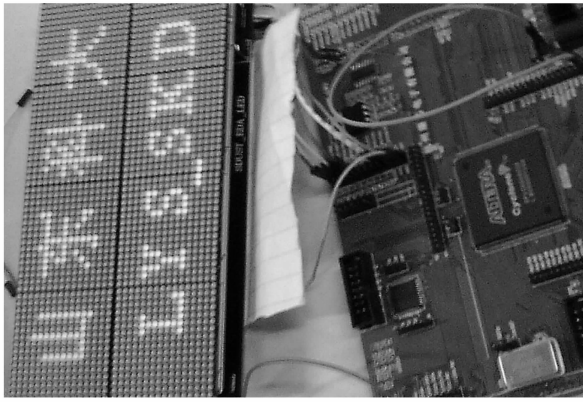
**Fig. 11　Test results**

1）In order to display stably, the time sequence must be precise, or display will be chaos.

2）The power driver matching is also important. Before the design, power circuit must be devise well in advance.

Design process and concrete procedures of LED display based on FPGA are introduced in the paper. In addition, the results of software simulation are presented clearly. In practical applications, this design can work effectively and steadily and meet the project's needs.

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