Portable Distortion Degree of Measuring Apparatus

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Abstract – Distortion is a technical indicator in the field of common voice signal processing. The design is a portable distortion degree tester, based on Field-Programmable Gate Array (FPGA, EP2C20) as the core, using harmonic analysis method which better solve the distortion problem of accuracy. It can achieve the signal transformation from the time-domain to the frequency-domain, and is widely used for signal spectrum analysis. All the components used in the design are low power, high performance, low drift and industrial grade components. The reference voltage sources of ADC and DAC have identical performance of high stability, high precision. The clock is the precise stable clock with FPGA temperature compensation. This project can get the cost-effective, high-precision, low power and portable design goals.

Key words – *distortion degree*; *FPGA*; *measuring apparatus*

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1 Introduction

In electronic technology, in addition to the widely used sinusoidal signal, we also use a variety of non-sinusoidal signals, such as language signals, music signals, image signals, cable signals, radar signal and data transmission signals and so on. In the signal generation or transmission process, no matter what kind of signals will always deviate from the ideal conditions, which may be larger or smaller than the standard signal characteristics[1]. In order to check and improve the performance of signal transmission, it is particularly important to study and measure the distortion.

Distortion is a significant technical indicator in the field of the common signal processing, radio and electrical measurements. In the radio measurement test, the accurate measurement of many parameters will involve the distortion measurements. To reduce the error of different test instrumentations and improve the accuracy of testing, we must lower the distortion of the signal source. At present, according to measurement principle the distortion equipment can be divided into two broad categories: fundamental and harmonic suppression method analysis. Fundamental suppression method is used in the general distortion of analog meter, which will produce a relatively great error; In contrast, harmonic analysis can better solve the distortion problem of accuracy, which is used to assure the content of each harmonic using the frequency analyzer and calculate the waveform distortion[2].

In many electronic devices, we can analyze the performance of equipments by checking the signal changes before and after the signal transmission. With the development of electronic technology, there will be higher requests for the distortion meter, for example, small size, light weight and automation, in order to improve the measurement speed, widen the scope of the frequency and range, and improve the measurement accuracy. In short, we make a new challenge in view of the above innovative point.

2 The block diagram and system solutions

The design is a portable distortion degree tester, based on FPGA (EP2C20) core and the harmonic analysis method. We can obtain the distortion degree of the input signal by the high-speed ADC samples which will store the sampling data in the internal RAM of the FPGA, and the internal implementation of Fast Fourier Transform (FFT) algorithm.

The distortion degree tester principle diagram based on FPGA design can be seen in Fig. 1.

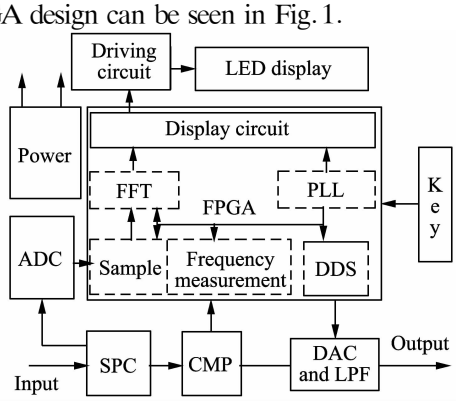

Fig. 1 Program block diagram

Firstly, the input signal through the automatic gain amplification can obtain the input signal fundamental frequency by the precision frequency in the FPGA[3]; Secondly, according to the requirements of fundamental frequency and the ADC sampling, we will get the ADC sampling clock by using Direct Digital Synthesis (DDS) principle[4]; Thirdly, the input signal is sampled and the sampling data will be stored in the internal RAM of the FPGA; Fourthly, we can obtain every harmonic component by the internal implementation of FFT algorithm the FPGA[5]; Lastly, we will calculate the distortion by the internal implementation of FFT in the FPGA and display in

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the 4 LED digital tube.

Also, we generate the standard sine signal by the principle of DDS, the DAC (DAC8820: 16 bits, 8 MHz) and low-pass filter (LTC1569-2)[6].

All the components used in the design are low power, high performance, low drift, industrial grade. The reference voltage sources of ADC and DAC have such performance of high stability, high precision. The clock is the precise stable clock with FPGA temperature compensation. This project can get the cost-effective, high-precision, low power and portable design goals.

3 Key modules analysis

3.1 Distortion test

In the fields of digital signal processing, FFT is the necessary premise of digital spectral analysis, which is the basic operation from time domain to frequency domain. Using IP Core of FFT we can realize FFT algorithm[7]. This method has high efficiency, high speed, short cycle, flexibility, etc. Because of the strong plasticity of IP core, it will increase the flexibility of chips.

The input signal is sampled 64 points per week. Using a 64-point Fast Fourier Transform (FFT) can get every harmonic amplitude component for the A_1, A_2, A_3, A_4, $A_5\cdots$ We can calculate the percentage of harmonic and fundamental distortion by

$$G_t = \frac{\sqrt{A_2^2 + A_3^2 + A_4^2 + A_5^2 + \cdots}}{A_1} \times 100\% . \quad (1)$$

The simulation waveform is followed in the Fig. 2.

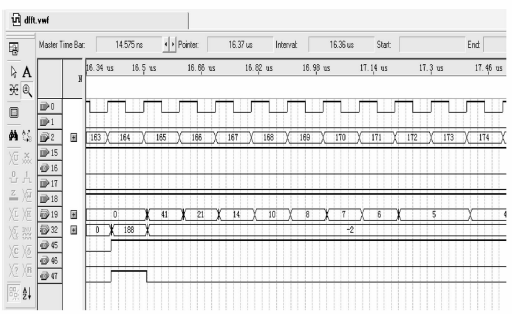

Fig. 2 Simulation waveform of FFT

In FPGA, the IP core can realize the Fast Fourier Transform[8]. It can achieve the signal transformation from the time-domain to the frequency-domain, which is widely used for signal spectrum analysis. At the same time, the IP core of FFT also makes comprehensive analysis of the simulink result[9]. After the comprehensive compilation, the engineering will generate Matlab files based on FFT nuclear generating contains, which can get the engineering testing result through Matlab. Application of IP core can design different performance requirements of Fourier transform processing module, shorten the development cycle, and save the cost. The IP core of FFT can conveniently and flexibly realize FFT algorithm by setting different parameters and structures of the IP core.

The IP core of FFT has been widely used in the field of digital signal processing, for example, different algorithms of FFT and FFT models to achieve optimization and so on. Most importantly, its performance is excellent. As a result, we have made the design based on the superiority of FFT which has reduced a lot of our design work.

3.2 Equal precision frequency test

TCLK is the signal (f_x). BCLK is the 10 MHz standard signal (f_s). CL is the test door control signal. START is the test allowing signal. The test allowing signal will count for input signal (N_x) and standard signal (N_s), the error of input signal is not ± 1, and standard signal is $1/(10 * 106)$ which are independent of the input signal frequency[4].

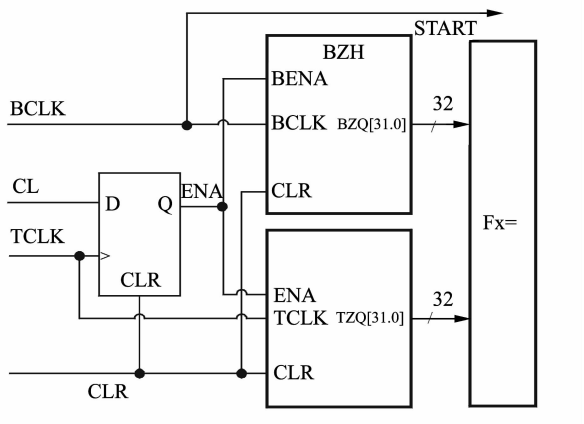

Fig. 3 Implementation diagram of equal precision frequency test

In a time of preset door, the count of the input signal is for N_x, and the standard signal is for N_s. The frequency can be got easily as

$$f_x = \frac{f_s}{N_s} N_x . \quad (2)$$

The realizing diagram of precision measurements in the FPGA is shown in the following Fig 4.

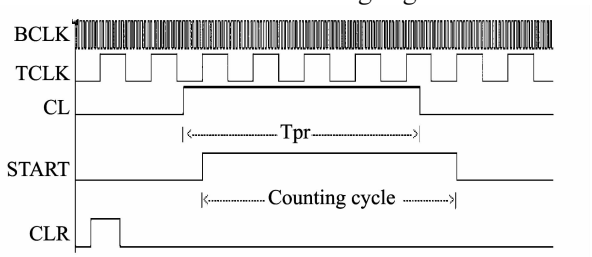

Fig. 4 Simulation waveform of equal precision frequency test

3.3 The reference signal synthesis

Recently, DDS has been a new method of frequency synthesizer. DDS direct digital frequency synthesizer is shown in Fig. 5. It consists of the phase accumulator, phase modulator; waveform data look-up table (ROM), amplitude modulator, which are the digital part of the DDS, analogy converter (DAC) and low-pass smoothing filter (LPF). And the digital part can all be realized in the

FPGA, which has the functions of numerical control frequency synthesis, sometimes collectively called "NCO".

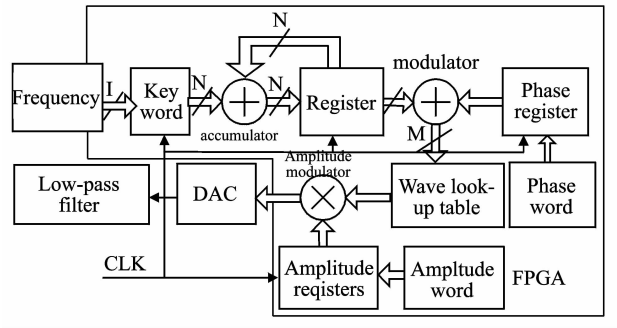

Fig.5 DDS principle diagram

The phase accumulator is the core of DDS, which can complete the phase accumulation function. Accumulator input is based on the frequency control word $B_{\Delta\theta}$ which can be calculated from Eq.(3)

$$B_{\Delta\theta} = 2^N \cdot \frac{f_{\text{out}}}{f_{\text{clk}}}. \tag{3}$$

Besides, the frequency accumulator will not be interfered after through a set of synchronized registers when the frequency word changes. Waveform look-up table (ROM) can complete the conversion from the phase to the amplitude. The input is the output of phase modulator, which is also the address of the look-up table values; the output is the waveform amplitude, which can convert the analogy signal through a multiplier for amplitude modulation and the DAC.

4 Function and index

4.1 Function

The design can measure the distortion degree of the input signal, complete the testing and display of the frequency, and generate the benchmark 1kHz sinusoidal.

4.2 Index

1) Input signal: 0~100 kHz periodic signals, 10 mV ~2 V.

2) The distortion degree: 0~99.99%.

3) Frequency: 0~100 kHz, error <0.1%.

4) Output signal: the benchmark 1 kHz, 2 V sine signal, the distortion degree <0.1%.

5 System test plan

First of all, SMT-200 test detectors test a string geophone tester for 5 times. Then using the portable distortion degree tester tests the same string geophone tester for 5 times. The accuracy of the portable distortion degree tester can be given through the comparison of them and the test dates are illustrated in Tab.1.

SMT-200 test is a standard measuring instrument of the distortion degree. By comparing, the result of portable distortion degree tester is basically the same with it. As a result, it can better solve the distortion problem by measuring the content of each harmonic.

From the measurement index, two measurement results are basically the same in spite of a little error, which may be due to the internal temperature compensation[10]. The problem is the distortion of the first test. The data is numerical, but the following one is more stable. So, to solve this problem, we must test again after the first time.

Tab.1 Instrument performance comparison chart

Tester	Time				
	1	2	3	4	5
SMT-200 tester	0.06	0.06	0.06	0.06	0.07
Portable distortion degree tester	0.07	0.07	0.06	0.06	0.06

Through observation data, we can draw the conclusion: the index test and test results are basically the same.

6 Summarization

In a word, this design has the following innovative points: ①Obtaining the input signal fundamental frequency by equal precision frequency test and generating the sine benchmark signals by DDS. ②Getting every harmonic component by the internal implementation of FFT algorithm and calculating the distortion degree in FPGA. ③ Battery-power, portable function and low-power consumption.

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