Multi-seed-encoding BIST Design with Low Power Consumption Based on the Folding Counter

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Abstract – In this paper, by using the folding counter and linear feedback shift register, a new vector generator is proposed. The decisive testing patterns are generated by using the selected fold distance. Then the folding counter seeds are encoded by the specialized seed encoder and clock gating, the ineffective patterns do not act upon the circuit under test, these testing patterns are designed to form a pseudo single input change set, so as to lead to prominent decreases in power consumption and redundant testing patterns generated by different seeds, without losing stuck-at fault coverage. Experimental results based on ISCAS'85 benchmark circuits demonstrate the efficiency of the approach.

Key words – *Folding counter*; *pseudo single*; *power consumption*

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1 Introduction

Pseudorandom testing pattern generator is usually adopted in Built-In Self-Test (BIST) because of the fewer hardware area overhead and higher fault coverage under limited input testing patterns. However, the number of testing patterns to diagnose the remainding difficult-testing faults will be too large to be used practically. So, the decisive pattern test set, e.g., fold set, which is simple and effective, is used to cover the difficult-testing faults, as shown in the approach of Ref. [1].

In the current integrated circuit, the clock signal is connected to the circuit through a clock tree, which is formed with clock buffers. The clock tree provides enough power and control the clock offset within a determined range. Because of the changes of the clock signal during system operation, power consumption increases due to the clock tree. It means that the reduction of redundant switching of the clock tree will lower the power consumption. On the other hand, as shown in Ref. [2], the switching activity of the circuit under test (CUT) during test application can be as high as 200% that in normal mode, because the functional input vectors applied to the circuit during the normal mode have significant correlations while pseudorandom testing patterns have not. It leads to a prominent increase in power consumption[3-5].

According to the above mentioned facts, this paper focuses on the reduction of power consumption by modifying the testing clock and improving the correlations between the testing patterns.

2 The basic BIST structure

The method for low power consumption comes from the idea of shielding ineffective testing patterns[1], as shown in Fig. 1. When the effective patterns are applied to the CUT, the clock signal is enabled; otherwise, clock signal is disabled for the ineffective patterns. Therefore, the power consumption due to the clock tree and the application of testing patterns by shifting into scaning path can be reduced.

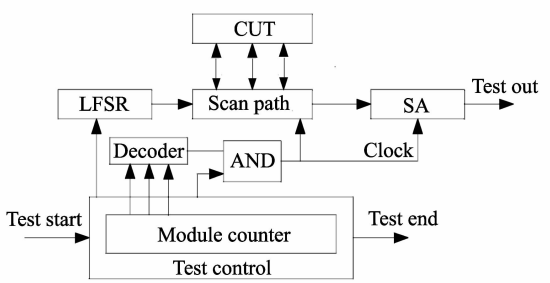

Fig. 1 BIST structure with clock gating

As shown in Fig. 1, the design of the decoder is decisive, for the clock signal is triggered by the output of decoder. The estimation of the efficiency of testing patterns is performed with a concurrent fault simulator and fault

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drop. When a testing pattern diagnoses extra faults, the output of the encoder will enable the clock signal, otherwise, the testing pattern is considered as ineffective and the clock signal is invalid. At the same time, the decoder detects the output of the module counter, so as to classify the effective testing patterns and its number as an on set and others an off set.

An example is given in Tab.1. Preceding three patterns can detect new faults, while the pattern which has sequence number 3 cannot. The maximal sequence number of those patterns which can detect new fault is recorded, e.g.,2 or 5 in Tab.1, and all the patterns whose sequence numbers are bigger than the maximal number, e.g., 3 and 6, 7, will be forbidden from applying to the CUT by the disability of the clock signal. It means that the patterns 0, 1, 2, 4 and 5 are classified as on set, while the patterns 3 and 6 as off set.

Tab.1 An example of test set

Serial number	Test pattern	Number of diagnosed fault
0	000	16
1	001	9
2	010	4
3	011	0
4	100	3
5	101	1
6	110	0

3 Methods of the Johnson counter

3.1 Theory of the Johnson folding counter

The Johnson folding counter is also named programmable Johnson folding counter, which has a state-shifting function, as shown in Eq.(1)[6]. The value of the function depends on the states of the counter and shifted distance. Using an original state $S \in \{0,1\}^n$,an $n+1$ state sequence $F(0,S),F(1,S),\cdots,F(n,S)$ is generated. The state $F(i,S)$ is similar to the state $F(i+1,S)$ for the preceding i bits, except that the remaining bits are inversed. The inversion is triggered only by the position j and shifted distance i .

$$inv(i,j)=\begin{cases} j \text{ if } j<1 \\ i \end{cases} \quad \begin{matrix} (1\leqslant j\leqslant n,0\leqslant i\leqslant n) \\ \text{else} \end{matrix}, \quad (1)$$

Assume $x \in \{0,1\}^n$ is a vector $x = x_1x_2\cdots x_i\cdots x_n$. Lets ${}^{-j}x_i$ denote a logical NOT operation to x_i , If j is an even number, ${}^{-j}x_i = x_i$; others ${}^{-j}x_i = \overline{x_i}$. Lets $F(k,x)$ denote k times fold calculation of x , as shown in Eq.(2).

$$F(k,x) = ({}^{-inv(1,k)}x, {}^{-inv(2,k)}x,\cdots, {}^{-inv(n,k)}x). \quad (2)$$

For example,

$x = 1001, k = 3, F(3,x) = {}^{-1}1\ {}^{-2}0\ {}^{-3}0\ {}^{-3}1 = 0010.$

3.2 Folding and decisive BIST

In this section, a new type of generator, called folding set generator is introduced. The generator is similar to the pseudo-pattern generator with an LFSR, and a folding controller is added to the output of the generator to modify bit flow and generate folding sets. All decisive testing patterns can be embedded into the processes of the folding set generation.

The folding set is a new set, which can be formed by half-and half folding an ordered set $T \in \{0,1\}^n$. A simple example is shown in Fig.1. An initial vector can be used to figure out a sequence of $n+1$ vectors, where for the the initial vector $S \in \{0,1\}^n$ can be folded times that the folding computation inverts the odd bits and retains the even bits from the first bit to the -th bit in s, in which the remaining bits from the -th bit to the last bit are regarded as a complete bit. A folding set of Fig.2 is shown in Tab.2.

Tab.2 Folding computing $S=000$

Folding compute	Folding vectors	Folding times
$F(0,s)$	0000	0
$F(1,s)$	1111	1
$F(2,s)$	1000	2
$F(3,s)$	1011	3
$F(4,s)$	1010	4

Compared to the classical generators, the folding set sequence produced from a single initial vector (seed) is rather short, and it is very unlikely that a complete set of decisive vectors can be embedded into a single folding set sequence. However, as it will be shown later, it is generally possible to find a reasonably small number of seeds, so that the union of all the resulting sequences covers a given decisive test set. This supports an efficient implementation of decisive BIST, and in particular for the scan-based BIST the basic structure is very simple. As is illustrated in Fig.2, the pattern generator consists of a ROM (stored seeds), a shift register and a folding controller.

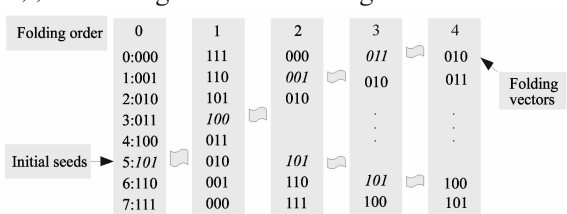

Fig.2 Folding vector forming

To generate a folding set to the CUT during BIST a seed is loaded into the shift register and the T-type flip-flop is reset. The bit and folding counters are initialized as "1" and "0", respectively. If the bit counter's value is smaller than the folding counter's, then output of the

comparator is "1", so that the state of the flip-flop is changed once after each clock plus, and the seed expanded by LFSR is alternately inverted and shifted into scanning path, otherwise the state remains. As soon as a folding pattern is completely shifted into the scanning path, the counter and T flip-flop are reset as "1", and the folding counter is activated. This procedure is repeated until the folding counter has cycled through all states and the next seed can be processed.

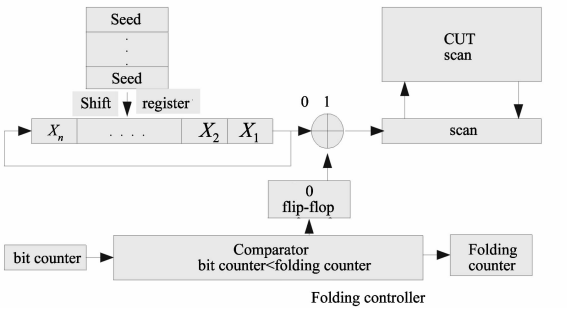

Fig. 3 Basic decisive BIST scheme of the folding controller

4 Clock and folding joint structure

Linear Feedback Shift Register (LFSR) is normally used as the Testing Pattern Generator (TPG) of the BIST, because of less hardware area overhead and better randomness of the pattern sequence[7]. The advantage of LFSR encoding is that it is only correlated with determining bits of the testing patterns, but is not related to those discretional bits. Thus, when the testing pattern includes large discretional bits, the testing set can be optimized by using the LFSR encoding and the Johnson folding counter. A flow chart of dual-encoding using the LFSR is shown in Fig. 4.

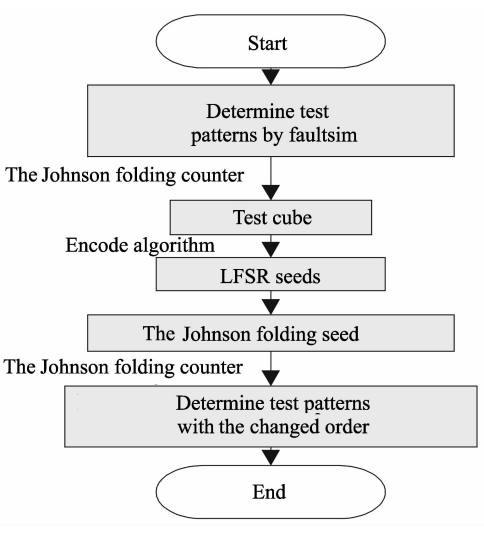

Fig. 4 Flow chart of dual-encoding

An example of the encoding procedure of the Johnson folding seed by the LFSR is shown in Fig. 5. A determined test cube is given in the left column, in which "x" denotes the discretional bit. With a corresponding seed "11" to the testing cube, the LFSR encoder, which has 2 stages, generates an output folding seed S = "110110". As an original folding seed of the Johnson folding counter, seed s is performed an operation with the equations (1) and (2), and therefore an extended fold vector set is obtained, as shown in the right column of Fig. 5. It obviously indicates that the determined testing cube is included in the fold state sequence, such as $F(0,S)$, $F(3,S)$ and $F(5,S)$. That is, it is enough if only the LFSR seed "11" is preserved for saving memory space.

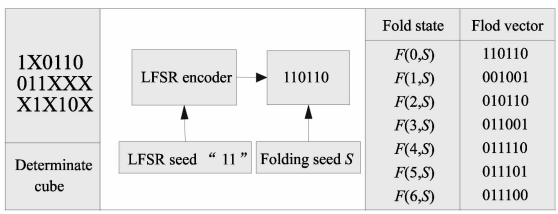

Fig. 5 An example of LFSR encoding

As shown in Fig. 6, LFSR has n stages, while the folding counter is an $(n+1)$ carry adder, which has a length of $\log_2(n+1)$. The output Y_i of the decoder is connected to a corresponding multi-selector MUX, i.e. the output Q_i of a flip-flop of LFSR is given to the CUT when Y_i is 1, while the output Q_{bi} is given when Y_i is 0, for $i = 1,2,\cdots,n$.

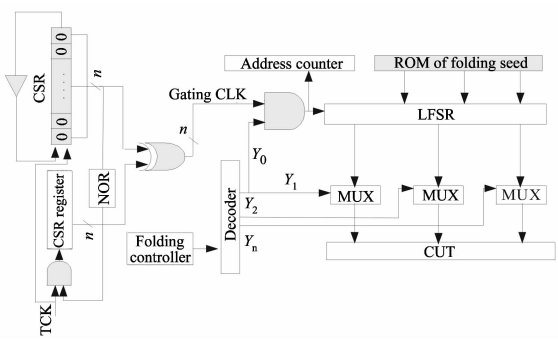

Fig. 6 Logic structure of multi-seed-encoding with clock gating based on the folding counter

When the counter is reset to zero, Y_0 is 1, while Y_i is 1($i = 1,2,\cdots,n$). At this time, CLK is allowed to apply to the LFSR due to the AND gate pass, and therefore a random testing pattern is generated by the LFSR. When the counter turns from 1 to n, Y_0 is 0, leading to the AND gate close and the disability of CLK. Thus, the LFSR doesn't work, i.e., the output testing pattern of LFSR will keep up until the counter is reset to zero again. During this period, the output signal $Y_i(i = 1,2,\cdots,n)$ of the decoder controls the MUX group so as to obtain an n extended test sequence which is also applied to the CUT. Here, design the BIST of adopts the test-per-clock structure.

Also, the order of the extended testing patterns is rearranged so that the change between any successive test patterns is only once. Tab. 3 shows an example, i.e. a folding seed "10111" is loaded into the LFSR and a testing

sequence with 6 extended patterns is obtained as shown in the right column ("fold vector") of Tab.3(a). After the redesign of the decoder, a rearranged sequence is obtained, as shown in the right column of Tab.3(b). It will greatly improve the correlation between the testing pattesns, and consequently reduce the power consumption. Because the change between the last pattern of the fold vector and the new folding seed sent to the LFSR is usually more than once, the total fold vector sequence is a pseudo single-input-change test set.

Tab.3 Normal fold vector and rearranged one

(a) normal fold vectors				(b) rearranged fold vectors			
Folding counter	Y_0	Y	Vectors	Folding counter	Y_0	Y	Vectors
0000	1	11111	10111	0000	1	11111	10111
0001	0	00000	01000	0001	0	01111	00111
0010	0	01111	00111	0010	0	01011	00011
0011	0	01000	00000	0011	0	01010	00010
0100	0	01011	00011	0100	0	01000	00000
0101	0	01010	00010	0101	0	00000	01000

5 Experimental results

The subjct in this paper is the benchmark circuits of ISCAS85, which are given by a gate-level netlist. The test definition is shown in Tab.4.

Tab.4 The basic information of ISCAS85 Benchmark

Circuit	Polynomial	Input	Fault number	Gate number
C 17	2,0	5	22	6
C 432	11,0,9,8,0	36	524	160
C 880	3,2,0,1	60	942	383
C 1908	13,0,11,0,0,9,0	33	1870	880
C 5315	91,0,87,0,76,53,0,21,0	178	5350	2307
C 6288	27,26,0,1,0	32	7744	2416

Because the ISCAS'89's benchmark circuits are very complicated, the paper uses the FAULTSIM simulation tools to test part of ISCAS'85's circuits. Simulations are carried out on the original LFSR and the proposed TPG is shown in Fig.4, and experiments are performed on some of the ISCAS'85's benchmark circuits. Firstly C++ is used to simulate the abovementioned test generation process, then the fold test set is obtained and applied to the CUT, to calculate the Weighted Switching Activity (WSA) and the Stuck-at Fault Coverage(SFC). Here, the WSA is used to describe the reduction of the total power consumption[3].

The first experiment focuses on the basic scheme of Fig.6 with the seed encoding. In this case the pattern generator requires a shift register of the same length as the scanning path. The LFSR for the random pattern generation is chosen of the same degree. Tab.5 shows the results.

Tab.5 Results for the basic scheme of figure 6

Circuit	LFSR length	Seeds number	ROM
C 17	5	2	10
C 432	36	16	109
C 880	60	38	213
C 1908	33	53	78
C 5315	178	63	896
C 6288	32	12	95

The experiment results are reported in Tab.6 and 7. It indicates that a comparative level of the total power consumption savings can be obtained, without lossof the SFC. In additionally, because an n-bit folding seed is extended by $n+1$ the patterns, the SFC will mainly depend on the preceding seeds placed in the ROM of the folding seed (Fig.6). Tab.7 gives an illustration of ISCAS'85's benchmark circuits. For most of the circuits, the SFC is beyond 90% when the preceding 30 seeds are used. After the extension of the preceding 30 seeds, rest can be extended by the fold distance or index, to concurrently meet the requirements of the power consumption and test time.

Tab.6 Experiment results of ISCAS'85's benchmark circuits

Circuit	SFC(%)	WSA		
		Without clock gating	This paper	WSA rate(%)
C17	100	2010	930	46.27
C 432	99.237	13 875	35 510	74.47
C 880	100	3 908 590	197 051	94.96
C 1908	99.492	7 927 530	1 800 200	77.29
C 5315	98.876	10 217 305	3 487 425	80.86
C 6288	99.561	15 843 201	9 641 946	60.92

Tab.7 Effect of the preceding folding seeds on the ISCAS'85's circuits

Circuit	SFC(%)				
	Preceding 5 seeds	Preceding 10 seeds	Preceding 15 seeds	Precedin 20 seeds	Preceding 30 seeds
C 17	100	–	–	–	–
C 432	33.51	73.63	98.67	99.23	–
C 880	13.24	43.75	78.69	99.25	100
C 1908	11.43	21.08	53.44	83.06	99.49
C 5315	5.62	13.89	42.45	86.71	98.876
C 6288	0.33	46.48	55.54	67.66	99.561

It can be observed that for all the cases a reasonably small number of seeds are sufficient to guarantee complete fault coverage. However, the long scanning chains lead to a considerable amount of overall storage for the larger cir-

cuits. To efficiently reduce the storage of seeds relying on seed encoding for folding seeds with respect to this problem, the experiments are repeated for the scheme of Fig. 6. Tab. 8 shows the results and compares them with the results achieved by competitive approaches published in Ref. [8]. Tab. 8 shows that the number of ROM is less than that in Ref. [8] and the SFC remains unchanged mainly.

Tab. 8 Comparison of that in Ref. [8] with that in this paper

Circuit	Reference[8]				This paper				ROM Rate	SFC Rate
	LFSR	Seeds	ROM	SFC (%)	LFSR	Seeds	ROM	SFC (%)		
C 17	2	5	15	100	2	2	10	100	0.67	0
C 432	9	22	186	99.57	8	16	109	99.23	0.59	−0.1
C 880	11	50	254	100	8	38	213	100	0.84	0
C 1908	15	64	91	99.41	12	53	78	99.49	0.85	0.1
C 5315	15	78	1024	98.35	12	63	896	98.876	0.86	0.1

6 Conclusion

The proposed BIST design with the low power consumption consists of a folding counter and multi-seed-encoding LFSR structure. Under the control of the clock, ineffective patterns are forbidden from applying to the CUT. On the other hand, the LFSR is firstly used as an encoder to make the folding seed, then as an encoder to generate extended testing patterns according to the decoding of the folding seed orderly. Moreover, by redesigning the decoder, a pseudo single-input-change test set is obtained. Relying on the control of the clock and the utilization of the testing patterns, the power consumption is greatly reduced.

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