High-precision grating sensor demodulation device's network interface based on DM9000A

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Abstract: High-precision fiber Bragg grating sensor demodulation instrument with wide-range dynamic scanning can effectively improve the measuring range of the optical fiber grating sensor. Ethernet communication module is an extremely important part of the high-precision grating sensor demodulation device. Network interface based on Ethernet control chip DM9000A is used to send and receive the Bragg grating sensing pulse. The network transformer YL18-2050S is used to convert and filter the pulse from network. The transmitting and receiving program of grating demodulation, hardware circuit of Ethernet transmission interface are designed. The experimental results show that the network interface can achieve accurate and real-time transmission of the grating sensing information at high speed.

Key words: DM9000A; network interface; grating sensing

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0 Introduction

There is a continuous growth of research interest in fiber Bragg grating (FBG) components for telecommunication, and they have been widely used in optical sensors and optical communications due to their promising performances such as electro-magnetic immunity, compactness, remote sensing, ease of fabrication and wavelength selectivity[1]. Using the method of real-time tracking of the sensing fiber grating reflection spectrum, the high-precision grating sensor demodulation devices network interface based on DM9000A effectively solves the problems of low accuracy caused by nonlinear filtering of intensity modulated fiber grating demodulation method, and significantly improves the fiber grating sensor measuring range. So the desiged system has broad application prospects. Ethernet technology, with advantages of flexible connection, excellent openness and compatibility, high efficiency, low cost and high speed, is widely used in a variety of computer networks, and still keeps developing[2]. The transmission of fiber Bragg grating sensing information in this paper focuses on the data link layer, using user datagram protocol (UDP) and address resolution protocol (ARP).

1 System architecture

The main device Ethernet control chip DM9000A[3] is used to implement the transmitting and receiving of fiber Bragg grating sensing information, and network transformer YL18-2050S is mainly used to realize the conversion and filtering of grating sensor pulse. The network interface sends data to the computer for further processing, which includes the real-time sensing fiber grating reflection spectral data, scanning voltage of the tunable filter and etalon transmission spectrum. Dynamic and static strain will be measured by computer according to the sensing fiber grating spectral peak position and its actual sampling time, the center wavelength of the Fabry-Perot (F-P) etalon and characteristic wavelength of Mag Flag. Field-programmable gate array (FPGA) configures DM9000A internal registers through the external data and address bus to complete DM9000A initialization and makes data transceiver keep in waiting state after system powered on. FPGA sets sending and receiv-

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ing status of the network interface chip to complete the mutual exchange of grating demodulation information between FPGA and Ethernet by setting DM9000A internal status registers. Fig. 1 shows a schematic diagram of the experimental setup.

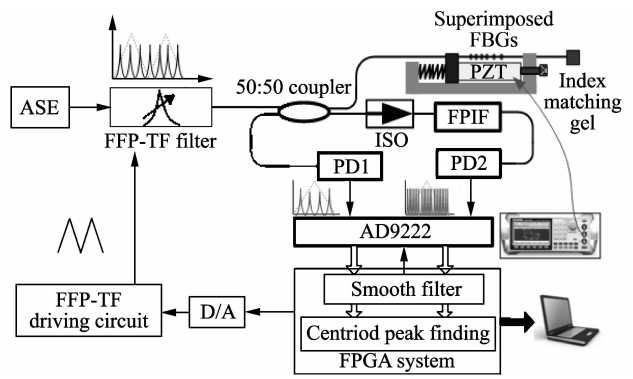

Fig. 1 Experimental setup for high-precision grating sense demodulation device

1.1 Introduction to DM9000A

DM9000A[4] is a high-speed Ethernet controller chip produced by Davicom Semiconductor Inc., which implements the functions of Ethernet media access layer (MAC) and physical layer (PHY). These functions include MAC data frames' assembly/split and transceiver, address recognition, cyclic redundancy check (CRC) encoding/check, MLT-3 encoding, receiver noise suppression, pulse shaping output, timeout retransmission, link integrity test, signal polarity detection and correction. DM9000A consists of a data transmitter, a receiver, a register, 16 Kb SRAM and 10/100 PHY. It supports a variety of interfaces (ISA bus) with the embedded microprocessor (MPU) and microcontroller. The advantages include small size, low power consumption, flexible configuration and ease of use.

1.2 Network transformer

The network transformer between Ethernet controller chip and RJ-45 in the design of network interface is YL18-2050S. The roles played by the network transformer[5] are as follows:

1) It is used to enhance the signal to increase the transmission distance;

2) It can isolate DM9000A from the external to enhance the signal anti-interference ability;

3) They do not affect each other to protect system circuit when network port receives a different level signal and completes the transmission of the signal. Its specific connection is given in Fig. 2.

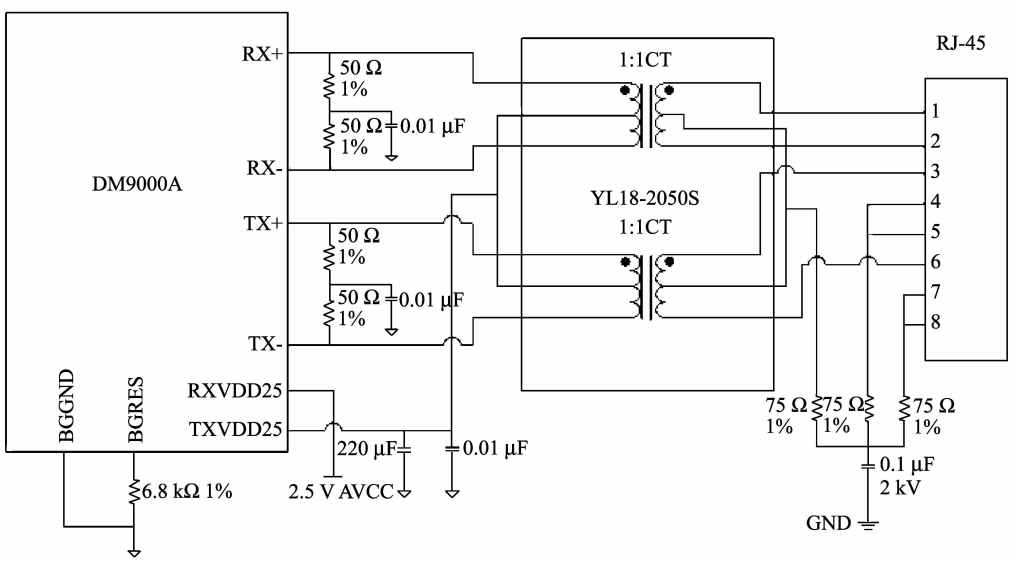

Fig. 2 Coupled isolation circuit

1.3 Interface circuit design

Data receiving and transmitting as well as DM9000A initialization are under the control of FPGA. XC4VLX25-10SF363I is chosen as a control element, which belongs to the Vertex ™-4 series of the Xilinx Com. FPGA and DM9000A are connected by 16 data bus and other control bus, etc., working in half-duplex mode. The read/write operations of DM9000A are controlled by CMD pin by default, and read/write signals and chip select signal are lowly active. The external bus of DM9000A can be connected directly to FPGA seamlessly. The hardware connection is shown in Fig. 3.

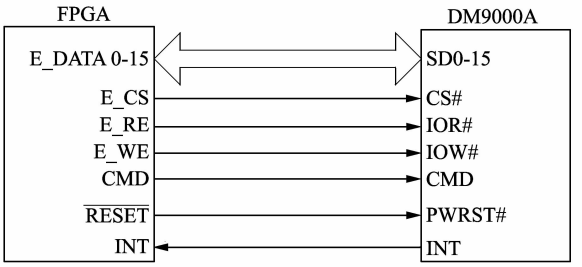

Fig. 3 DM9000A and FPGA connection diagram

2 FPGA program and protocol

FPGA control program is composed of three parts: Ethernet controller chip initialization, packet transmission and reception. The detailed program flow chart is shown in Fig. 4. According to different status and length, ARP protocol or UDP protocal is selected, and subsequently different operations are performed.

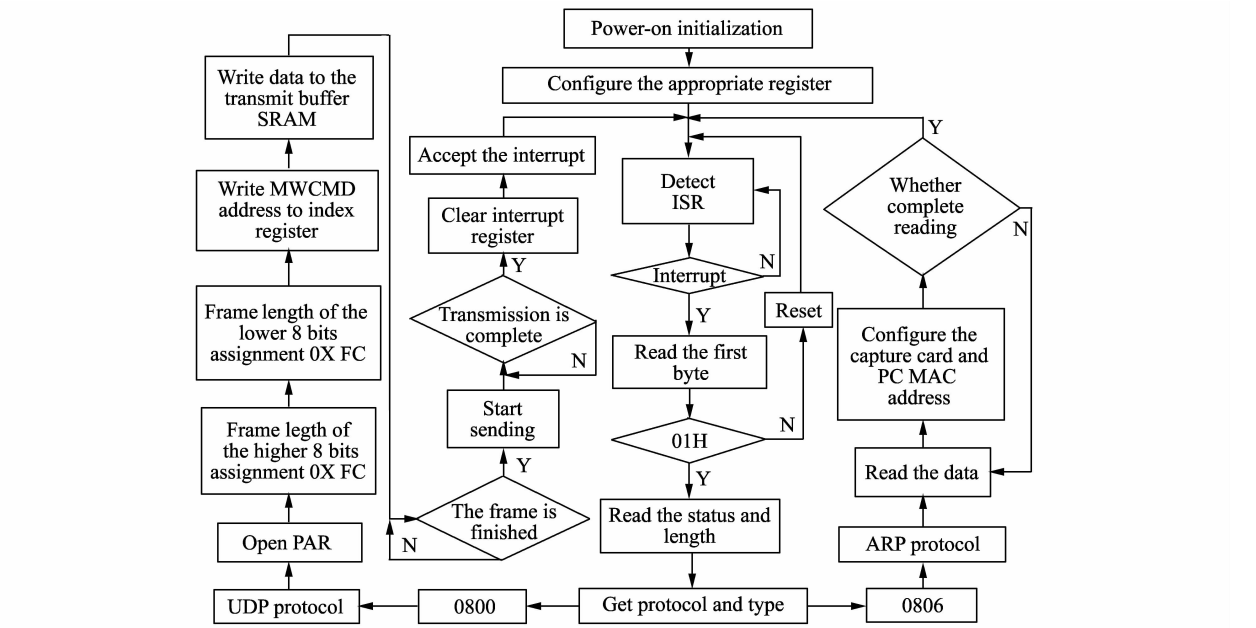

Fig. 4 Flow chart of FPGA program

2.1 DM9000A initialization

The initialization process of DM9000A is to set the internal control registers of DM9000A, which is completed through read/write operations by its external data bus and control bus under the control of FGPA. DM9000A initialization[5] steps are as follows: 1) DM9000A wakes up from sleep mode after power-on reset; 2) DM9000A is reset twice by softwave; 3) DM9000A work mode is set in normal mode; 4) The last of the sending state is removed; 5) Read/write address pointer automatical return function is enabled; 6) Network interface chip read/write interrupt is enabled; 7) The data reception function of DM9000A is openned.

2.2 Data packet transmission module

DM9000A internal data transmission buffer can store two frames of data at the same time, named frame I and frame II sequentially. The state control word is recorded in status register addressed 03H and 04H. Data transmission procedure is as follows: FPGA configures write register to transmit data frames to DM9000A transmitting buffer firstly. Data frame length of the higher 8 bits and the lower 8 bits of information are stored in the register FCH and FDH, respectively. The length of the frame should contain the MAC address segment of both the destination and source, and the total length of the valid data. PTS is the transmitting interrupt flag of interrupt service routine (ISR) register. When data transmission is completed, PTS = 0. Then FPCA clears the flag to send new data frame. DM9000A processes the data automatically, and sends it to Ethernet. Subsequently, DM9000A begins to send data of frame I, data of frame II is written to the transmission buffer simultaneously. Data frame's number continues to change according to repeated frame I and frame II in turn. DM9000A will produce an indication of the transmission completion interrupt signal when data transmission is completed if FPGA set bit[1] of interrupt mask register is high. During the process of transmission, FPGA can query TX1END bit[2] or TX2END bit[3] of the flag register to obtain the transmission state of data frames. The data transmission process is showo in Fig. 5.

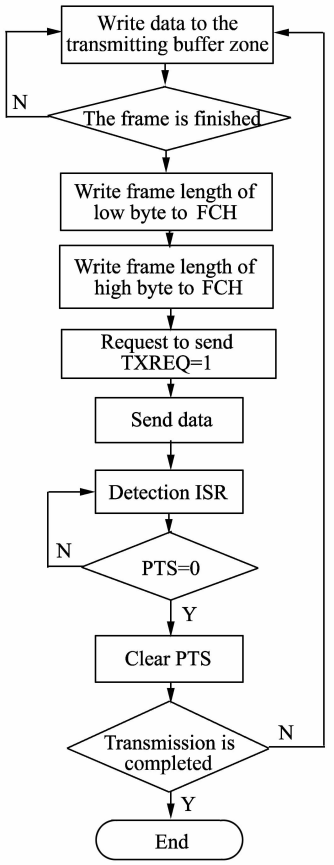

Fig. 5 Flow chart of DM9000A data transmitting process

2.3 Packet receiver module

DM9000A receiving buffer is a circular structure with starting address 0C00H. Packet receiving is actually the process of handling interrupts. An interrupt is generated to invoke packet reception program to deal with the reception of the packet when data arrives. The data receiving process is as follows: Firstly, FPGA checks the interrupt status register to determine whether there is an interrupt. If the new data is received, the PRS of the interruption status register will be set 0, and FPGA starts to read the data in receiving buffer. If the data of the first byte is 00H, it is indicated that there is no data. But 01H is opposite. If the first byte detected is other status, it means an abnormal state, so it is necessary to give a soft reset. According to the second byte of the data, correction of the received frame is determined. If it is correct, the third and fourth bytes are read to obtain the length of the data information. It can be seen whether the data frame is read solely according to the results. That the first byte of the data frame is 00H means all the data has been received completely. If an interrupt appears upon receiving a data, the interrupt mask register (IMR) PRM bit[1] should be set 1. FPGA can detect IMR flag bit to determine whether there is a new valid data frame. DM9000A data receiving process is shown in Fig. 6.

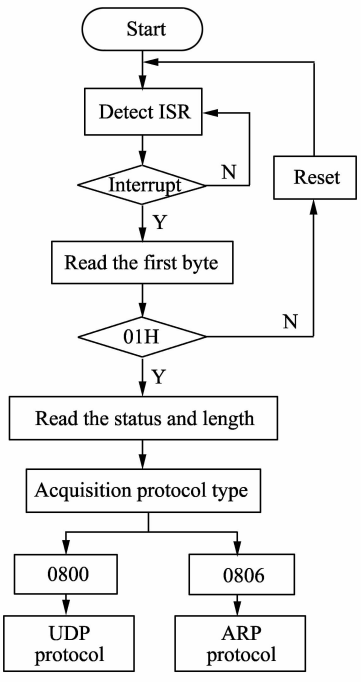

Fig. 6 Flow chart of DM9000A data receiving process

3 Results

To evaluate the performance of the designed system, a test is conducted in the following.

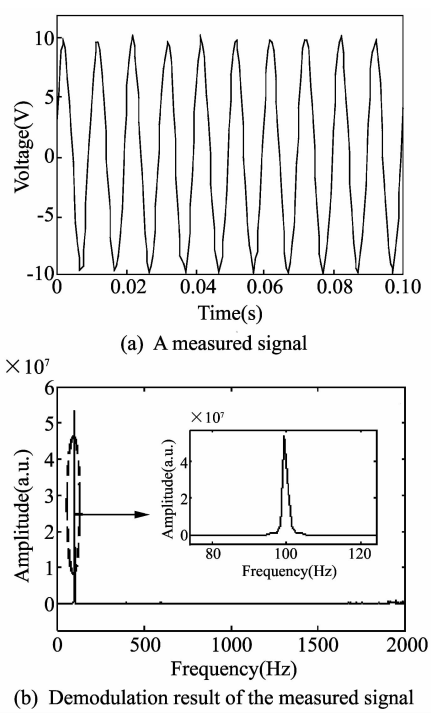

Fig. 7 Ethernet data spectrum received by computer

Using the network interface based on DM9000A, the tunable filter scanning voltage is sent. F-P etalon transmission spectrum and the sensing fiber grating reflection spectram are collected in real time in the grating demodulation system. Dynamic and static strain are measured by computer according to the sensing fiber grating spectral peak position and its actual sampling time, the center wavelength of F-P etalon and characteristic wavelength of Mag Flag.

Fig. 7 is a 100 Hz sine demodulation result of the dynamic strain signal, in which Fig. 7(a) is a 100 Hz time domain signal and Fig. 7(b) is a 100 Hz frequency domain signal demodulated result. It can be seen from Fig. 7 that the time domain and frequency domain spectrum can directly restore the original signal characteristics of dynamic strain.

4 Conclusion

This paper introduces high precision grating sensor demodulation device's network interface based on Ethernet control chip DM9000A and describes the principles of DM9000A operation mode and hardware interface with FPGA. The network transformer YL18-2050S and its hardware connection are given, and FPGA program and communication systems used in the design of the protocol are presented. Practice has proved that the network interface based on DM9000A can be applied to the grating sensing demodulation system, and it has the advantages of low power consumption, small size, stable operation, real-time high-speed signal demodulation.

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