Test system for miniature pulse-powered photoelectric invert switch based on CPLD

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Abstract: For electronic piezo gauge used for testing gun chamber pressure, its internal miniature pulse-powered photoelectric invert switch cannot often be powered up normally. To solve this problem, a test system for invert switch is presented to verify the reliability of the invert switch. The test system uses complex programmable logic device (CPLD) to control data acquisition of A/D converter and data storage of external flash memory, and then transmits the acquired data to a computer for data analysis and processing. The test system can provide the required sampling frequency of the signal in high temperature, normal temperature and low temperature environments, and the reliability of the invert switch can be verified according to the signal parameters. The results show that the test system has high precision and the tested invert switch has low power consumption and high reliability.

Key words: invert switch; storage measurement technology; complex programmable logic device (CPLD); test system

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0 Introduction

Low power design is desired by storage measurement technology[1-3]. A miniature pulse-powered photoelectric invert switch has been implemented and has become the key part of the power control unit of storage measurement system. It is a new switch that is suitable for volume production and without manual operation. It has the characteristics of low voltage actuation, low power consumption, small volume and time delay function[4]. In actual storage measurement, there were many failed tests because the test system could not be powered up normally by the invert switch. Considering the high cost of test experiments, it is necessary to verify the reliability of the invert switch[5-8].

1 Photoelectric invert switch

The miniature pulse-powered photoelectric invert switch is composed of photoelectric control module and CPLD control module. The functional block diagram is shown in Fig. 1.

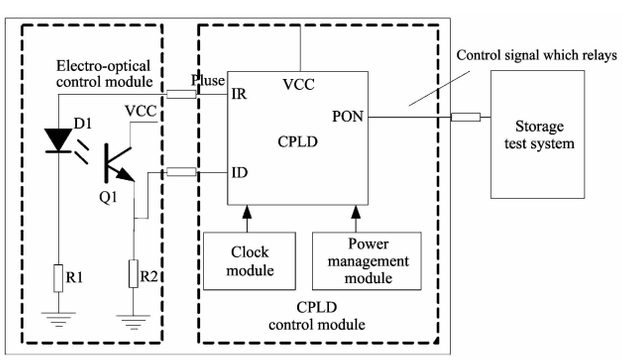

Fig. 1 Block diagram of miniature pulse-powered photoelectric invert switch

In Fig. 1, D1 is an infrared emitting diode, Q1 is a phototransistor, IR is pulse voltage signal, ID is the output signal of Q1 and PON is the delay signal of electrical control signal. To reduce the power consumption of the photoelectric invert switch, pulse-

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driven approach is adopted for infrared emitting diode in photoelectric control module.

2 Test system

2.1 Design of test circuit

The block diagram of test circuit for photoelectric control module signal ID is shown in Fig. 2.

It can be seen that the test system consists of analog-to-digital (A/D) converter, FIFO1, FIFO2, external static memory, high frequency oscillator, complex programmable logic device (CPLD) control module, power control module and serial communication interface. Among them, CPLD control module is the core. According to the needs of signal acquisition, the test circuit adopts two FIFO chips to implement the double negative delay function.

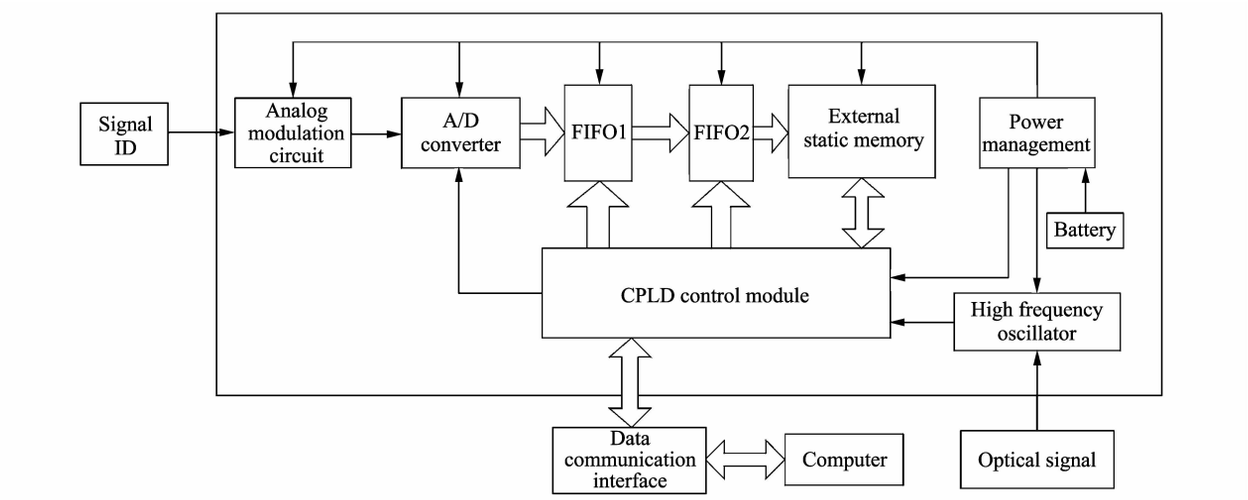

Fig. 2 Block diagram of test circuit for photoelectric control module signal ID

The working principle of test system is as follows.

The output signal ID of photoelectric controlmodule is an important parameter to be monitored. When the photoelectric control module is triggered by a external optical signal, the signal ID output by the photoelectric control module is sampled circularly and at the same time the acquired data are written into FIFO1. When the rising edge of signal ID arrives, the data in FIFO1 is imported to FIFO2 and the data in FIFO2 is to external static memory until the memory is full. At this time, data acquisition stops and the acquired data is waiting for being read from the static memory. When receiving a read command from the computer, the system begins to count until the data transfer is completed. Finally, if the computer needs to read the data again, it will send a read command and the test system will run as the above steps, or else, the test system will be reset or cut off.

2.2 Logic design of CPLD control module

High performance and low power CPLD EPM7128BTC100-4 belongs to MAX7000B series from Altera company. It is the core of the test circuit[8]. The block diagram of CPLD control module is shown in Fig. 3 and the schematic diagram is shown in Fig. 4.

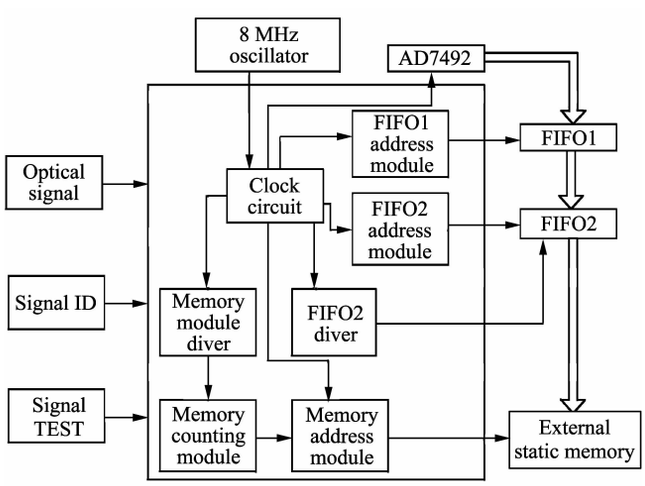

Fig. 3 Block diagram of CPLD control module

When the rising edge of trigger signal ID arrives, A/D converter begins to sample and the acquired data

is written to FIFO1 by write operation. Meanwhile, FIFO1 and FIFO2 push the address and then FIFO1 performs read operation and FIFO2 performs write operation. Afterwards, the static memory and FIFO2 push the address and FIFO2 performs read operation and static memory performs write operation. Consequently, the data are imported from FIFO2 to the static memory. When the static memory capacity is over 375 KB, a full count signal is sent and correspondingly the computer sends the read command to read the data again.

If signal TEST arrives, the test system will work as the same as the first step. A/D converter begins to sample again and the data are stored. Meanwhile, FIFO1 and FIFO2 begin to push the address. Afterwards, the data are read from FIFO1 and then written to FIFO2 . It is negative delay. Based on the same control principle, if there are 64 sampling points for FIFO2, when the rising edge of the trigger signal TEST arrives, FIFO2 and static memory begin to push the address. Meanwhile, begins to read the data and the static memory begins to write the data. The data in FIFO2 is the signal with arrow pulse peak before signal ID, and then adjacent wave signal is written into the memory. The 192 sampling points in all are stored in the memory, which are the signal ID peak and the adjacent wave signal. After that, the memory stops writing the data and waits for the next the rising edge of the signal TEST. Finally, the computer generates read signal and begins to read the data in the memory. When the memory is full, end signal is sent after the 1 000 th trigger signal.

In Fig. 4, clk module is responsible for controlling the address operation of FIFO1, FIFO2 and static memory and judging whether the static memory capacity is full.

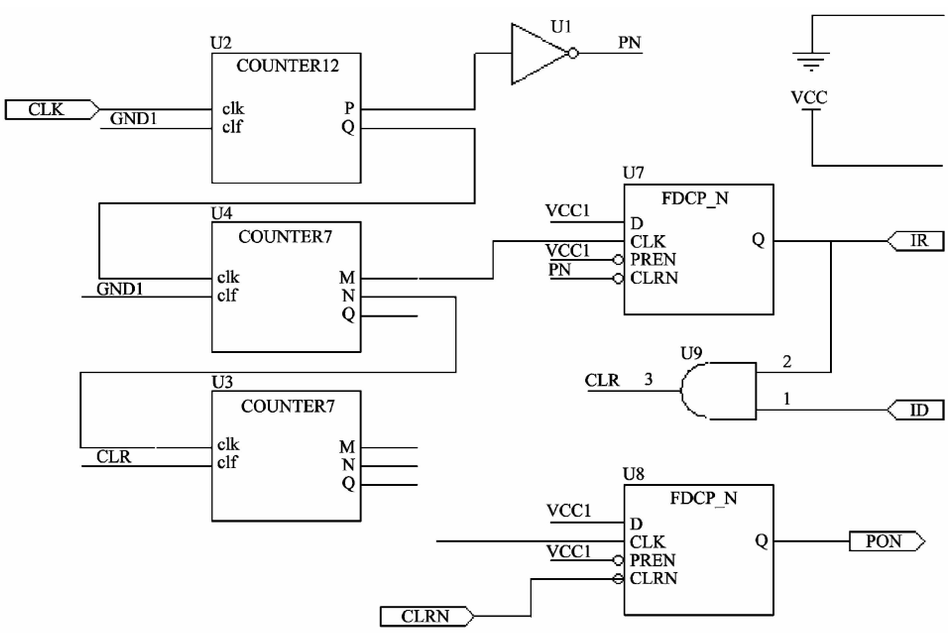

Fig. 4 Schematic diagram of CPLD control module

2.3 Simulation of signal ID

Quartus II is used for test system design and implementation. It is a synthetical PLD development software from Altera company with embedded synthesizer and simulator, which can complete the design process from design input to hardware configuration. Fig. 5 shows the CPLD timing.

For a practical pulse-powered photoelectric invert switch, the high level of signal ID should last 122 μs theoretically. Using the designed test system, the real high level of ID signal waveform is obtained as 120 μs, as shown in Fig. 6. The test result is very close to theoretical value 122 μs, which proves the reliability of the pulse-powered photoelectric invert switch used.

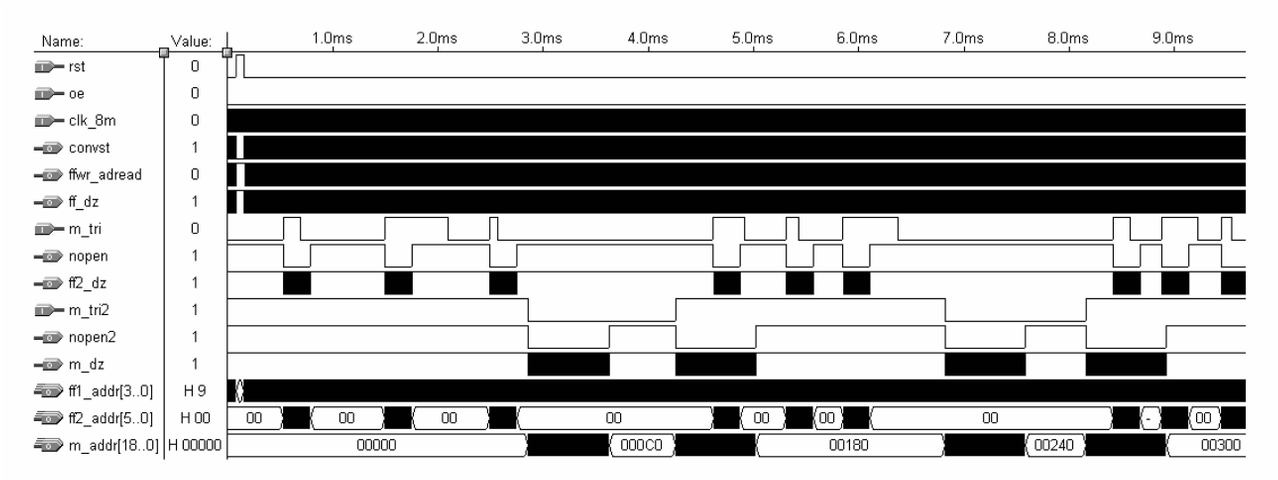

Fig. 5 CPLD timing

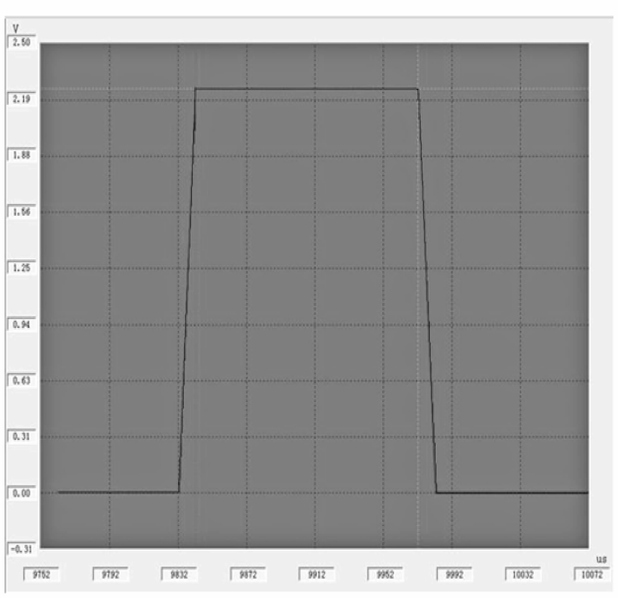

Fig. 6 Waveform of signal ID

3 Conclusion

This paper describes a test system for miniature pulse-powered photoelectric invert switch. Especially, the test system uses two FIFO chips to realize the double negative delay function, which provides a reference for the collection of narrow pulse signal. The test result proves the reliability of the invert switch.

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基于 CPLD 的微型脉冲供电式光电倒置开关测试系统

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摘 要： 针对放入式电子测压器在测试火炮膛压时，内部的微型脉冲供电式光电倒置开关无法正常上电的问题，设计了倒置开关的检测系统。该系统由 CPLD 控制 A/D 转换器的数据采集和外部闪存的存储，将采集的数据传输到计算机中进行分析处理。系统能满足高温、常温和低温环境下信号的采样频率，并可根据信号参数验证倒置开关的可靠性。试验结果表明，该检测系统精确度高，且被测倒置开关功耗低、可靠性高。

关键词： 倒置开关；存储测试；CPLD；测试系统

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