Multi-channel & high-precision data acquisition device for aerospace

ZHENG Yong-qiu(郑永秋)[1,2], REN Yong-feng(任勇峰)[1], LIU Xin(刘 鑫)[1,3], CHU Cheng-qun(储成群)[1]

(*1. Science and Technology on Electronic Test & Measurement Laboratory, University of China, Taiyuan 030051, China;*
2. Key Laboratory of Instrumentation Science & Dynamic Measurement (North University of China), Ministry of Education, Taiyuan 030051, China;
3. College of Electronics and Information Engineering, Taiyuan University of Science and Technology, Taiyuan 030024, China)

Abstract: This paper describes the detailed design of data acquisition device with multi-channel and high-precision for aerospace. Based on detailed analysis of the advantages and disadvantages of two common acquisition circuits, the design factors of acquisition device focus on accuracy, sampling rate, hardware overhead and design space. The mechanical structure of the system is divided into different card layers according to different functions and the structure has the characteristics of high reliability, convenience to install and scalability. To ensure reliable operation mode, the interface uses the optocoupler isolated from the external circuit. The transmission of signal is decided by the current in the current loop that consists of optocouplers between acquisition device and test bench. In multi-channel switching circuit, by establishing analog multiplexer model, the selection principles of circuit modes are given.

Key words: data acquisition; multi-channel; high-precision; analog multiplexer; field-programmable gate array(FPGA)

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0 Introduction

In the filed of aerospace measurement, it is crucial to acquiring the environmental parameters including temperature, pressure, vibration, humidity, acceleration and so on, which is the guarantee of success for the space flight experiment. Simultaneously, by analyzing the acquired data, adaptability and reliability of the aerospace equipment can be evaluated, which can support the development and improvement of equipment[1-2].

The data acquisition system with multi-channel and high-speed is a hot topic in parallel data acquisition technology[3]. The number of signal channels can range from tens, up to hundreds. If each channel is set to an A/D converter, it is unrealistic considering volume, power consumption and costs. It is practicable that all channels are time-share by analog multiplexer. But the problems resulting from multiplexers such as channel-to-channel crosstalk and transmission delay have been the constraints for the improvement of acquisition device. In this paper, we give the principles for the design mode of analog multiplexer[4-5].

In the field of aerospace measurement, the launching cost of launch vehicle is proportional to the weight, 100 million per one kilogram, while the success rate of the launching is inversely proportional to the weight. So the acquisition devices of aerospace equipment have the characteristics of micro-miniaturization, multi-channel, scalability, low power consumption, high precision and high reliability[6-7]. The project is presented based on this application background. Considering various factors, we give the optimization analysis and universal design of the acquisition devices. Field-programmable gate array (FPGA) is used as the control unit[8-9]. Compared with the micro control unit (MCU) and digital signal processor (DSP), FPGA will not be affected by instruction cycle based on very-high-speed hardware description language (VHDL) at high speed and efficiency of execution. All of its control logic is run on the hardware, with high clock frequency, small internal delay, programmable configuration flexibility, small size, low power consumption, and lots of available I/O ports. It can control sampling, processing, cache, transmission and communication in FPGA. Thus, for multi-channel parallel and high-speed data acquisition,

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Corresponding author: ZHENG Yong-qiu (zhengyongqiu86@163.com)

FPGA is preferred as the control unit.

1 Structure of data acquisition system

1.1 Form of circuit

There are two kinds of circuits for multi-channel signal input and acquisition, namely, synchronous acquisition circuit and asynchronous time-share acquisition circuit, as shown in Fig. 1.

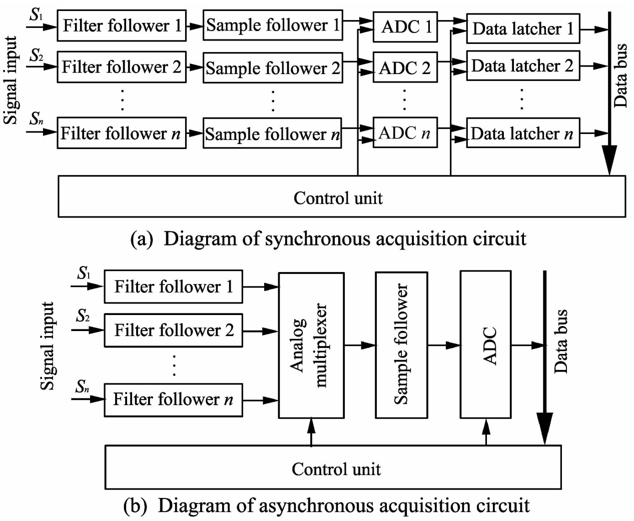


Fig. 1 Diagrams of multi-channel acquisition circuits

Each circuit has certain advantages and disadvantages. If we only consider accuracy and sampling rate, Fig. 1(a) is an ideal acquisition circuit. But considering the hardware overhead, it needs to set up a set of signal transmission and A/D converter for each input signal channel, which increases size, weight and power consumption. It is neither necessary nor economic. Furthermore, it is not desirable for too large volume occupied in the finite volume environment.

However, in practical applications, according to the test requirements and characteristics of the multi-channel input signal, the analog multiplexer is usually used for time-share acquisition and conversion, as shown in Fig. 1(b). It is a more reliable, more feasible and simpler way of working[10-11].

1.2 Mechanical card layers

The acquisition device consists of two card layers, with convenience to install, high reliability and scalability. The internal structure is shown in Fig. 2. The circuit boards for signal input and control are fixed in different card layers, respectively, which are connected via J80-ZK2/4 connectors. In control card layer, X1 interface is used for power input, start signal input, data transmission with the computer and configuring FPGA through joint test action group (JTAG) mode. X3 connector is used for transmission of data, command and status signals between the device and memory. X2 connector is used for external multi-channel analog signal input.

Taking into account thermal design of the product, a separate cooling aluminum plate is designed for four power supply modules W117/W137 with large volume, metal packaging F-1. The design increases the cooling area, and effectively reduces the impact on accuracy due to the rise of the devices temperature.

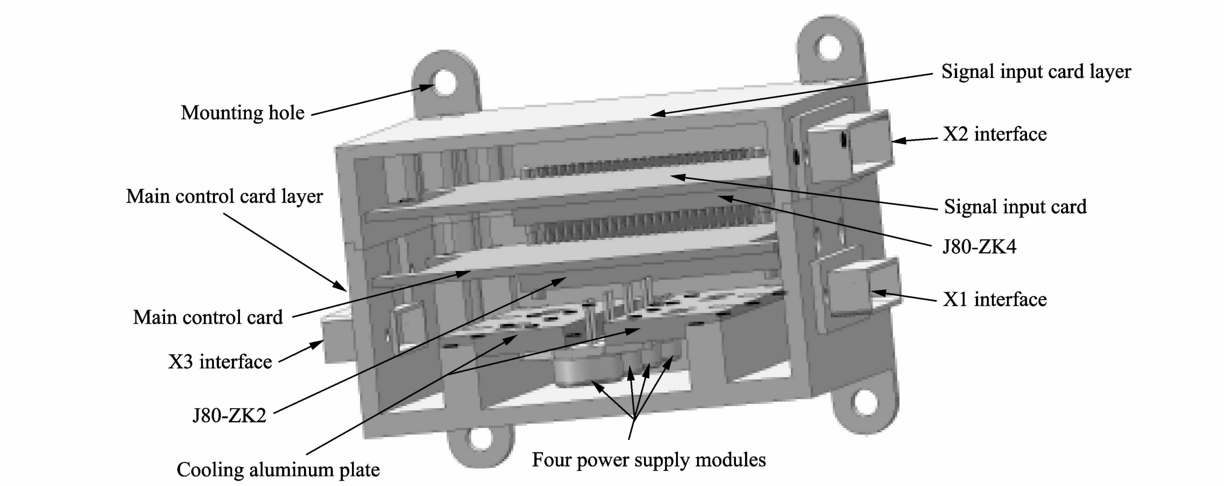


Fig. 2 Internal structure of acquisition device

2 Design of circuit

2.1 Functional modules

The design diagram of functional modules is shown in Fig. 3.

The main control card implements the following key functions: controlling ADC, encoding data in a frame and timing control. X1 interface receives various commands from the test bench, transmits real-time monitoring data to computer, reads out data of memory remotely, and importantly, provides power input; Memory is connected via X3 interface, through which data can be stored and read out.

The signal input card provides interface X2 for multi-channel analog signals input. Before analog-to-data conversion, analog signals will be adjusted through filter circuit, op-amp follower circuit, multi-channel switching circuit and signal conditioning circuits, etc.

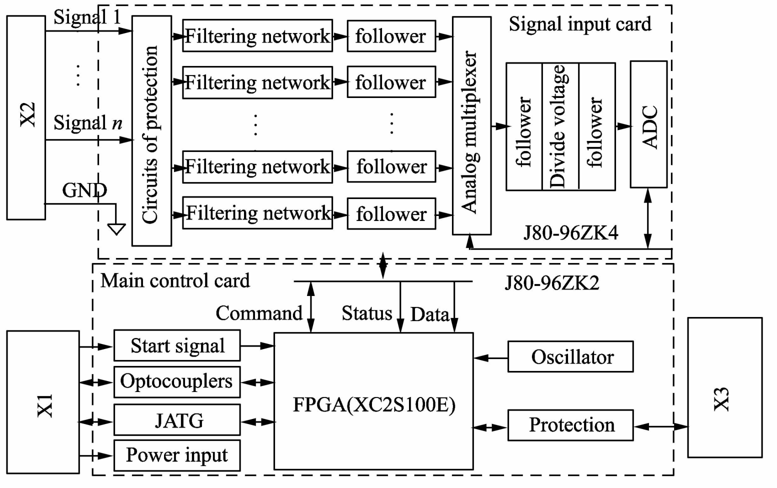


Fig.3 **Circuit diagram of the acquisition device**

2.2 Control mode

The control commands from the test bench mainly include control signal RD/WR, selecting signal CHOICE, data request signal REQUEST, and monitoring signal INSPECT, which are transported via interface circuits connecting with the test bench.

All the interface circuits between the acquisition device and the test bench are isolated from each other by the optocouplers. And thus when the external short circuit occurs, the operation of the internal circuit of the aircraft can not be affected. The interfaces of the acquisition device and the test bench are connected by the cables, so that a pair of optocouplers can form a current loop. The current in the loop is the pre-requisite of the signal transmission. The interface circuit of the optocouplers is shown in Fig.4, which is given when the direction of signal transmission is from the test bench to the acquisition device.

The acquisition device has six operation modes, S1 – S6, as shown in Table 1. Y indicates there is current in the current loop, while N is just the opposite. After aircraft takes off, the acquisition device will automatically works in S6 mode, which records state with low-power. In S1 – S4 modes, the data of memory chosen by CHOICE can be read out. The request signal REQUEST is given from test bench in pre-flight test or recovery test, while it is inactive when aircraft is in flight.

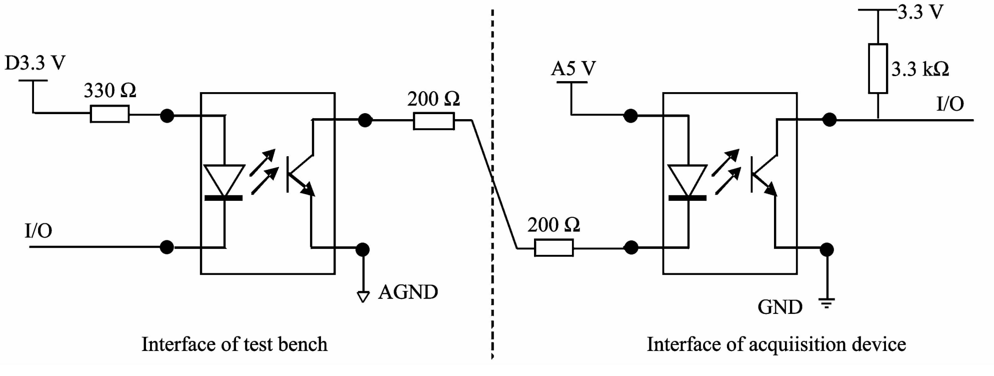


Fig.4 **Interface circuit of optocouplers**

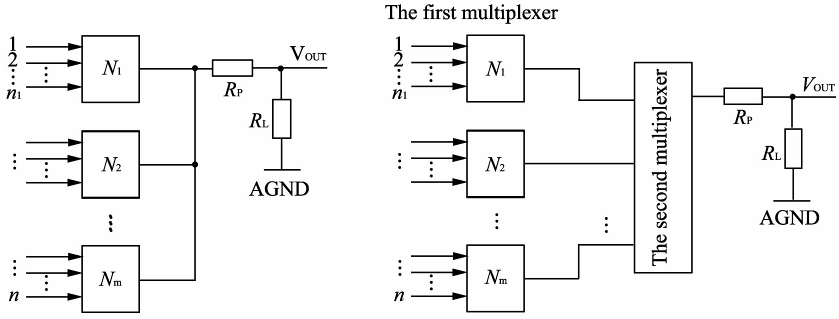
Table 1 Operation modes of acquisition device

Signal name	Read and write control	Memory select	Real-time monitoring	Data request	Status flag	Explanation
Flag	RD/RW	CHOICE	INSPECT	REQUEST		
Read	Y	N	N	Y	S1	1# memory chosen; read state; it is reading.
Read	Y	N	N	N	S2	1 # memory chosen; read state; pause reading
Read	Y	Y	N	Y	S3	2# memory chosen; read state; it is reading.
Read	Y	Y	N	N	S4	2 # memory chosen; read state; pause reading
Write	N	N	Y	N	S5	Write state; real-time monitoring for the data
Write	N	N	N	N	S6	Write state; no monitoring; no operating for optocouplers; low power

3 Design principle of multi-channel switching circuit

The multi-channel switching circuit uses analog multiplexer to save hardware cost and space. In order to improve the system accuracy of conversion, short conduction time is required to ensure fast signal transmission. The leakage current can be reduced to a minimum by small conduction resistance and large off resistance, which reduces the impact on signal transmission. The most important factor is settling time of the output signal is fast. Owing to conduction resistance and inter-electrode capacitance of analog multiplexer, there is a certain transition time, especially there is maximum difference between previous and present channels. It is equivalent to a step signal applied to input terminal of analog multiplexer, so that output terminal will also show the charging or discharging process of step signal. If the establishing process of step signal can not stabilize when ADC enters sample state and initiates a conversion, it will cause a conversion error. Even more, it will result in a reduction of ADC conversion accuracy when conversion error is greater than ±1 LSB (least significant bit). This is the reason of channel-to-channel crosstalk in analog multiplexer. Thus, the settling time of the output signal should be as short as possible, to ensure that the signal has stabilized before ADC sampling[4,12-13].

There are two combinations of analog multiplexer for multi-channel analog signals switching. Fig.5(a) is the combination of one stage, and Fig.5(b) is the combination of two-stage cascade switching circuit. Here are selection principles for these two combinations as follows.



(a) One order combination (b) Combination of two-order cascade

Fig.5 Two combinations of analog multiplexer

3.1 Principle of optimal accuracy

Fig.5(a) is the combination of one-order analog multiplexer, whose advantages include simple connection, easier achievement of control program, very low power consumption, low cost of hardware and space savings. But the equivalent resistance from a closed (is sampling) switch is the parallel result of all switch resistors. Thus, all the switch leakage current will flow through the sampled signal, which will cause conversion error.

Suppose n-channel signal input, the drain current of the switch is I_D, and the equivalent load is R_L. Then the number of the parallel resistors is $N_1 = n$.

The error caused by all the switch leakage current is

$$\Delta u_1 = n \cdot I_D \cdot R_L. \quad (1)$$

Fig. 5(b) is the combination consisting of two-order cascade analog multiplexer. Compared with Fig. 5(a), the power consumption, cost of hardware, space required and operation difficulty of control program have increased. The time of transmission delay is more than the sum of the two multiplexers'. While its main advantage is to reduce the sampled signal error due to the leakage current.

In such a case, the same as n-channel signal input, the number of the parallel resistors is

$$N_2 = \frac{n}{m} + m - 1, \quad (2)$$

where m is the number of one-order analog multiplexer, $\frac{n}{m}$ is the number of transmission switch in each one-order multiplexer.

Through the derivative of Eq. (2), we get the least number of one-order analog multiplexer $m = \sqrt{n}$, Thus

$$N_2 = \sqrt{n} + m - 1 = 2\sqrt{n} - 1. \quad (3)$$

The error due to all the leakage current of transmission switch is

$$\Delta u_2 = (2\sqrt{n} - 1) \cdot I_D \cdot R_L. \quad (4)$$

obviously, $\Delta u_1 \geqslant \Delta u_2$.

3.2 Principle of time accuracy

Owing to the presence of switch resistance, source capacitance and drain capacitance, the switch is equivalent to a RC charge-discharge circuit when one switch is turned on. The time of charge or discharge causes transmission delay of the signal. The simplified model of the analog multiplexer is shown in Fig. 6.

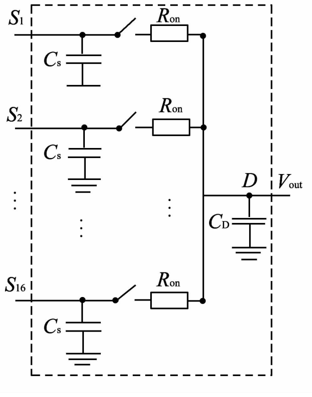


Fig. 6 Simplified model of the analog multiplexer

In Fig. 6, C_S and C_D are source capacitance and drain capacitance, respectively; R_{on} is the conduction resistance. The input signal has been loaded before the switch is turned on, so the switch conduction is mainly affected by drain capacitance C_D. For convenience of analysis, we only consider the charge process from the lowest level to the highest level, and the discharge process from the highest level to the lowest level. Suppose the peak-to-peak value of input signal is V_E. The charge process of output terminal V_{out} of the analog multiplexer is

$$V_{out} = V_E(1 - e^{-\frac{t}{R_{on}C_D}}). \quad (5)$$

The discharge process of output terminal V_{out} of the analog multiplexer is

$$V_{out} = V_E e^{-\frac{t}{R_{on}C_D}}. \quad (6)$$

The time constant of one-order combination is $\tau = R_{on}C_D$. The two-order combination is the concatenation of two analog multiplexers. The source capacitance of the second multiplexer must be considered. In result, the time constant will be $\tau = (R_{on} + R_{on})(C_D + C_S + C_D)$.

Of the analog multiplexer ADG506, known conduction resistance R_{on} is 600 Ω, source capacitance and drain capacitance are equal, $C_S = C_D = 50$ pF. The peak-to-peak value of input signal is 5 V. In the ideal case, the process of charge and discharge of output terminal V_{out} of the two combinations are shown in Fig. 7.

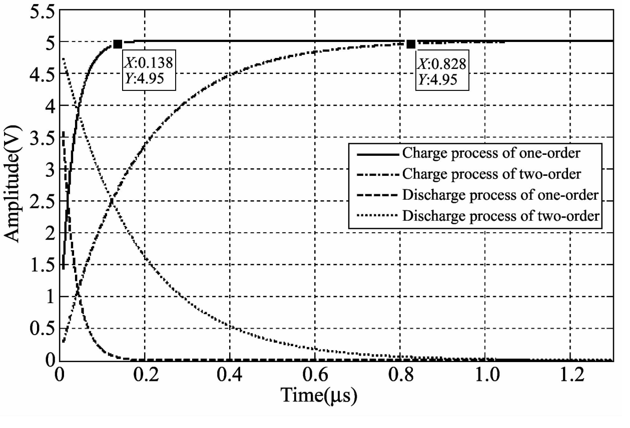


Fig. 7 Process of charge and discharge

As can be seen in Fig. 7, under the ideal conditions, the settling time to 1% of the output signal by one-order analog multiplexer is 138 ns, while that of the two-order cascade analog multiplexer is 828 ns. Considering the crosstalk between channels, the external interference and other factors, the settling time will be longer.

4 Conclusion

In conclusion, we analyze the design of multi-channel data acquisition for aerospace. Combining with practical applications, we give the feasible and reliable designs including the form of the circuit, mechanical structure and multi-channel switching circuit, which achieve comprehensive optimization of the acquisition device. The acquisition device can expand the number of signal input channels, in order to acquire more environmental parameters, which bring a great deal of flexibility to multi-channel data acquisition for the aerospace. The future trends in the field of aerospace test are more channels, higher speed and higher precision. The switching of more channels and high speed of sampling rate will bring more problems such as channel-to-channel crosstalk, oscillation caused by load change when analog multiplexers are switched and when op-amps drive capacitive load. These problems have been serious restriction on the improvement of accuracy and stability. So, there is still a lot of room for improvement of acquisition device in the future.

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